

FIG. 1

$$\begin{array}{ccccccc} \mathbb{Z}^{(n)} & \mathbb{Z}^{(n)} & \mathbb{Z} & \mathbb{Z} & \mathbb{Z}^{(n)} & \mathbb{Z}^{(n)} & \mathbb{Z}^{(n)} \\ \text{free} & \text{free} & \text{free} & \text{free} & \text{free} & \text{free} & \text{free} \\ \text{rank } n & \text{rank } n & \text{rank } 1 & \text{rank } 1 & \text{rank } n & \text{rank } n & \text{rank } n \\ \text{free} & \text{free} & \text{free} & \text{free} & \text{free} & \text{free} & \text{free} \\ \text{rank } n & \text{rank } n & \text{rank } 1 & \text{rank } 1 & \text{rank } n & \text{rank } n & \text{rank } n \end{array}$$


Fig. 3

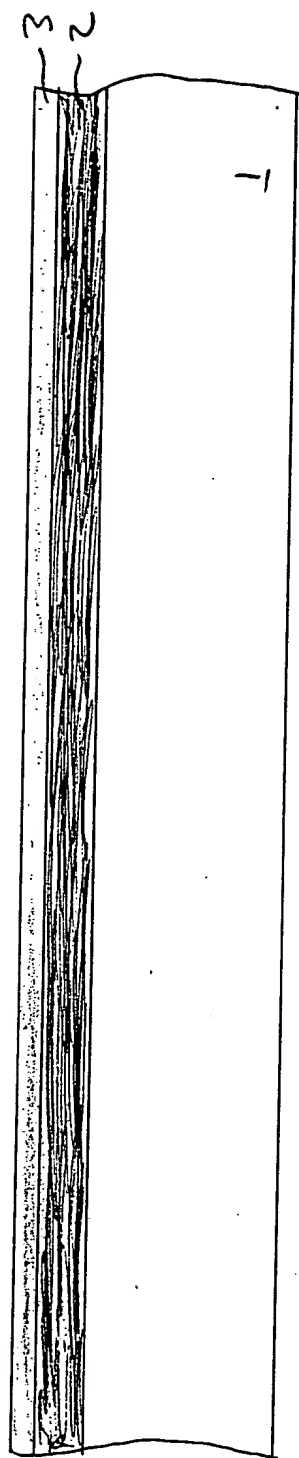


FIG. 4A is a perspective view of a first embodiment of a device 100. The device 100 includes a main body 1 and a first end 2. A first layer 4 is disposed on the first end 2 of the main body 1. The first layer 4 is a thin, elongated, rectangular layer that is attached to the first end 2 of the main body 1. The first layer 4 is shown in a perspective view, indicating its thickness and its position relative to the main body 1.

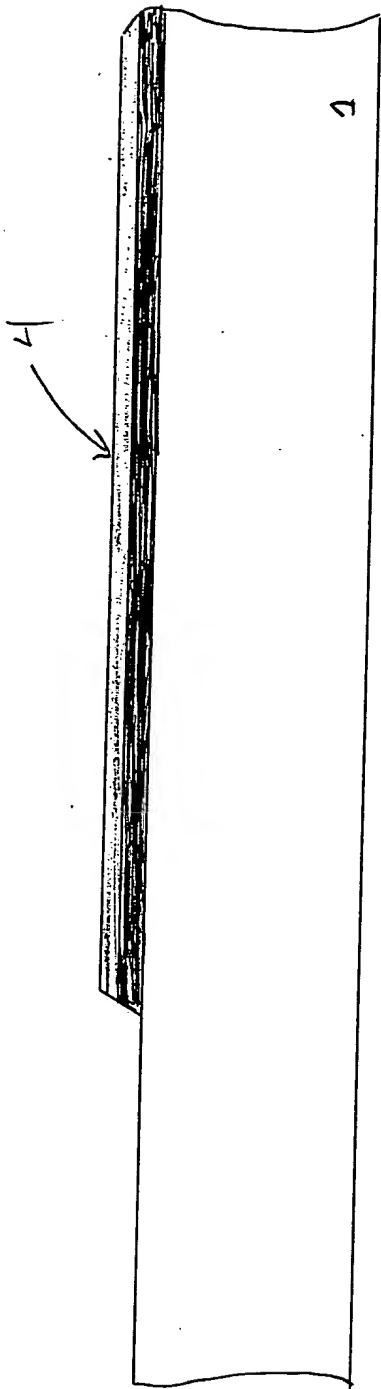


FIG. 4A

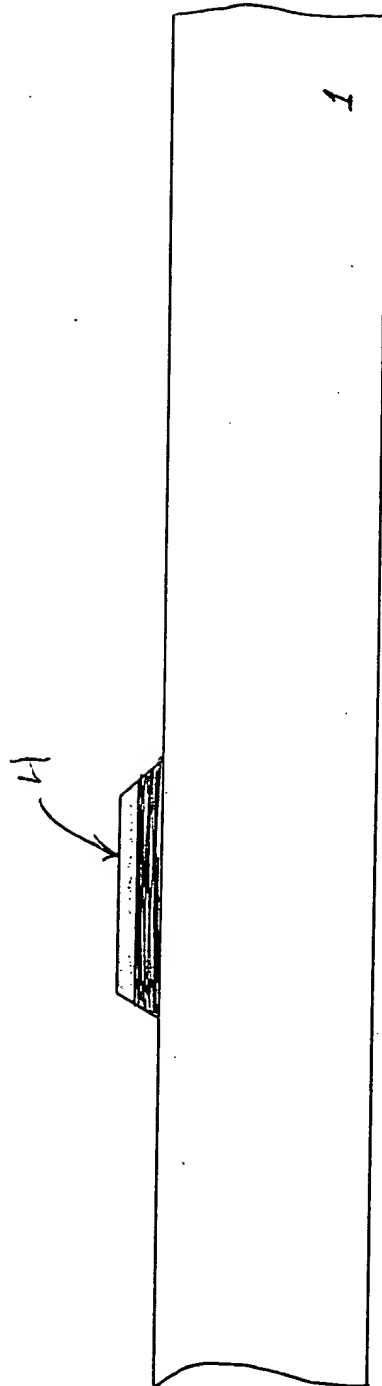


FIG. 4B

FIG. 5A

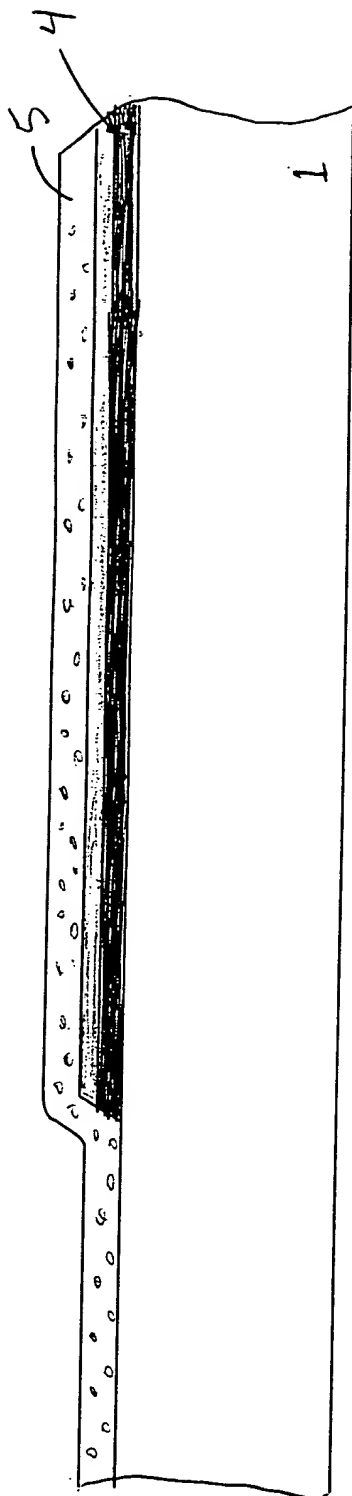


FIG. 5A

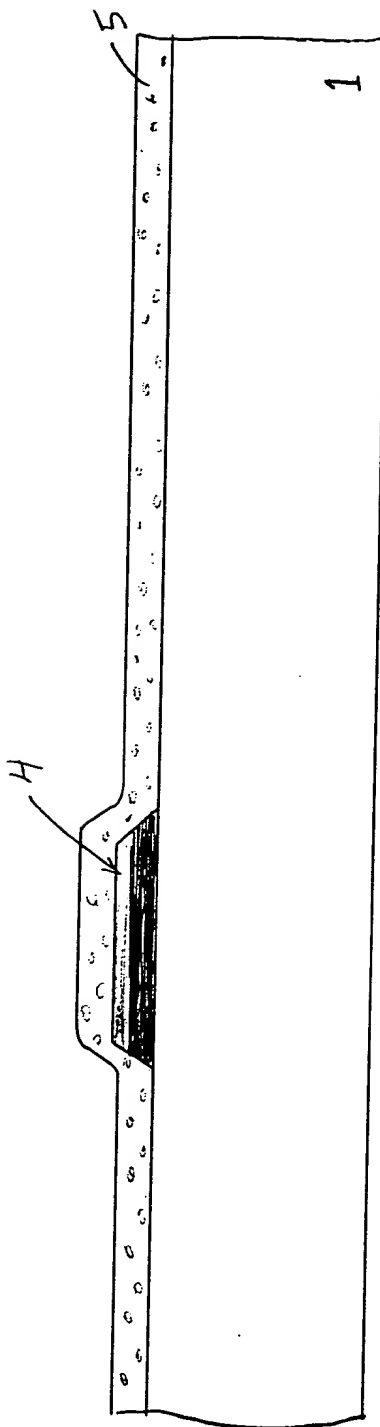


FIG. 5B

FIG. 6A is a cross-sectional view of a device 100, showing a substrate 1, a layer 4, and a layer 5. The layer 4 is a thin layer, and the layer 5 is a thicker layer. The device 100 is shown in a cross-sectional view, with the substrate 1 at the bottom, the layer 4 in the middle, and the layer 5 at the top. The layer 4 is a thin layer, and the layer 5 is a thicker layer. The device 100 is shown in a cross-sectional view, with the substrate 1 at the bottom, the layer 4 in the middle, and the layer 5 at the top. The layer 4 is a thin layer, and the layer 5 is a thicker layer.

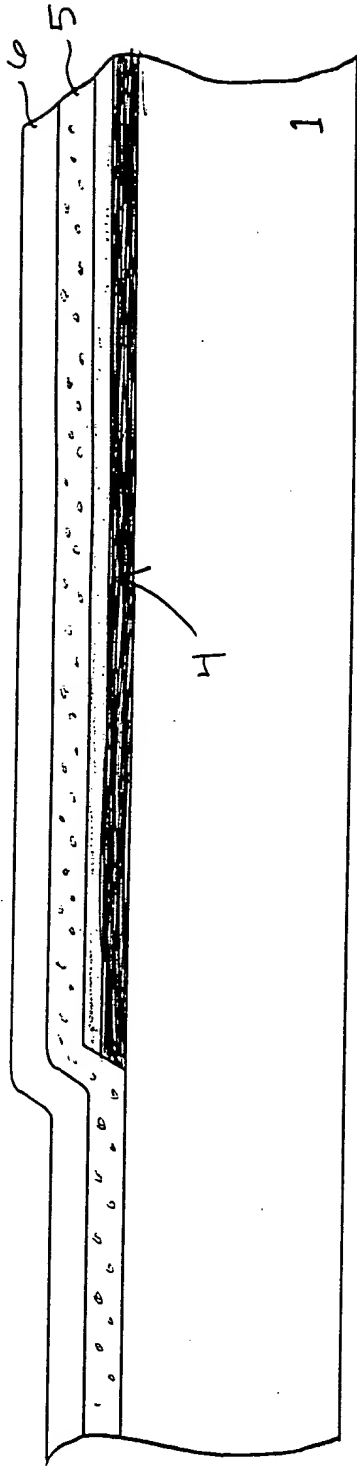


FIG. 6A

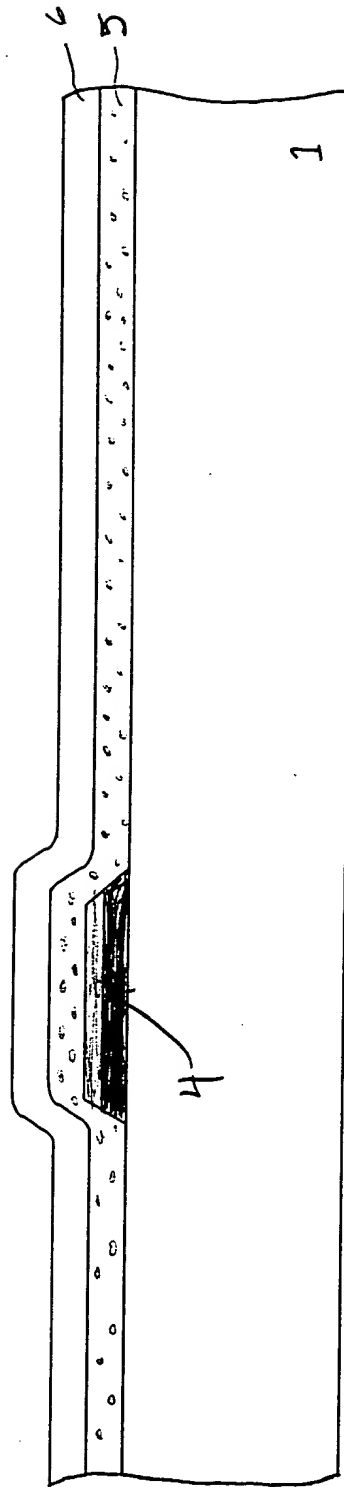


FIG. 6B

FIG. 7A is a cross-sectional view of a device 100, showing a substrate 102, a layer 104, and a layer 106. The device 100 is shown in a cross-sectional view, with the substrate 102 being a thick, solid layer. Layer 104 is a thin, patterned layer on top of the substrate. Layer 106 is a thin, solid layer on top of layer 104. The device 100 is shown in a cross-sectional view, with the substrate 102 being a thick, solid layer. Layer 104 is a thin, patterned layer on top of the substrate. Layer 106 is a thin, solid layer on top of layer 104.

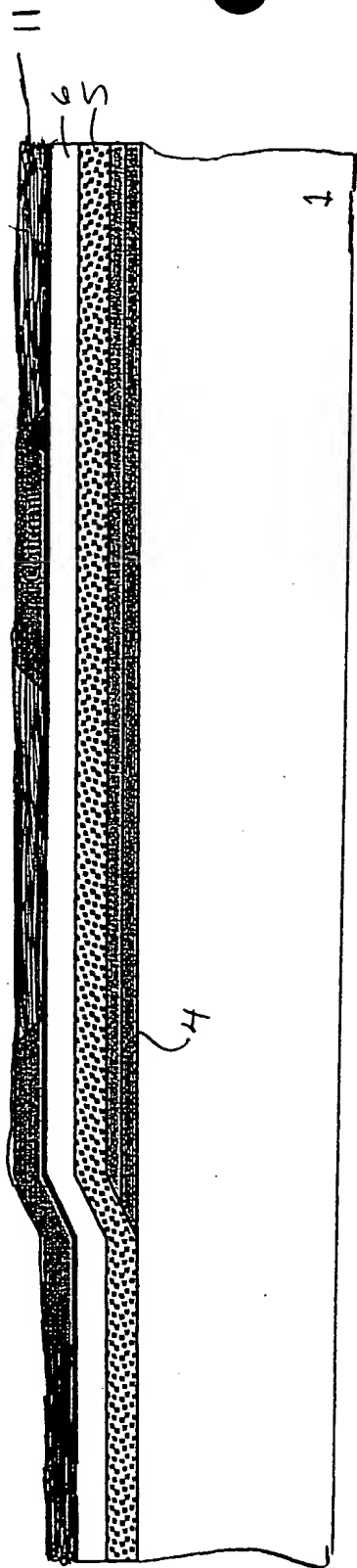


FIG. 7A

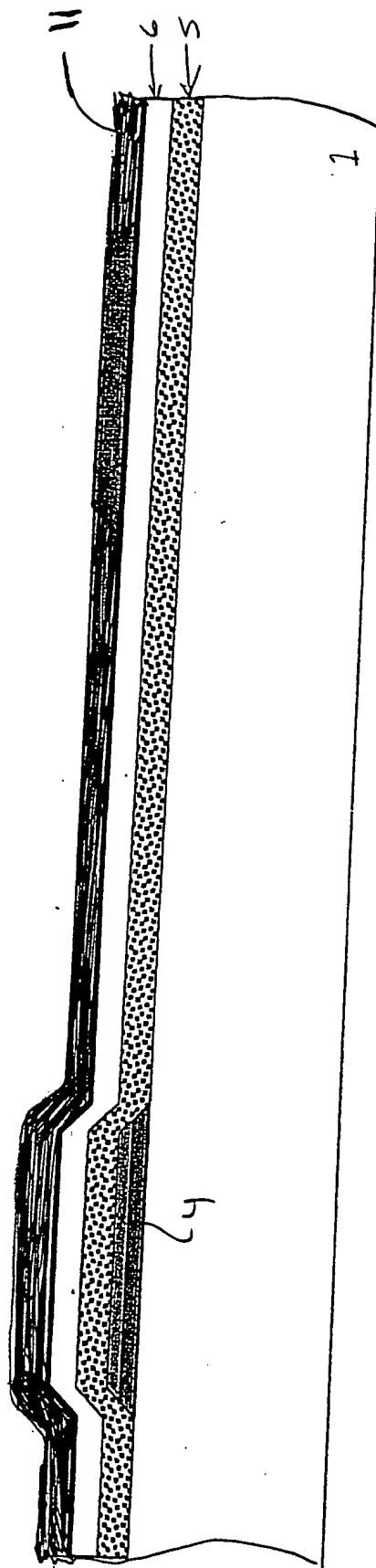


FIG. 7B

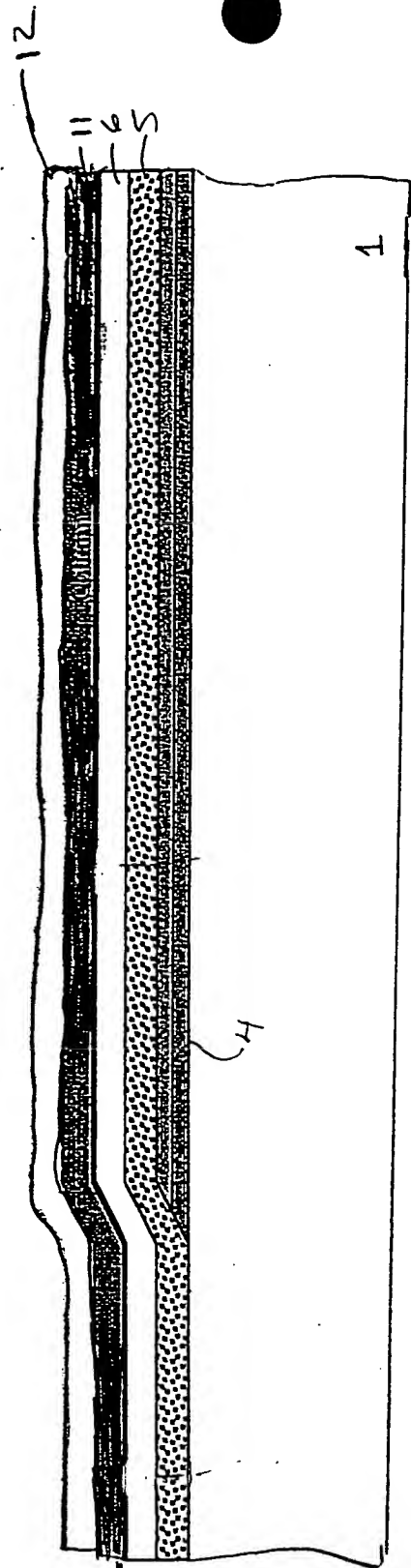


FIG. 8A

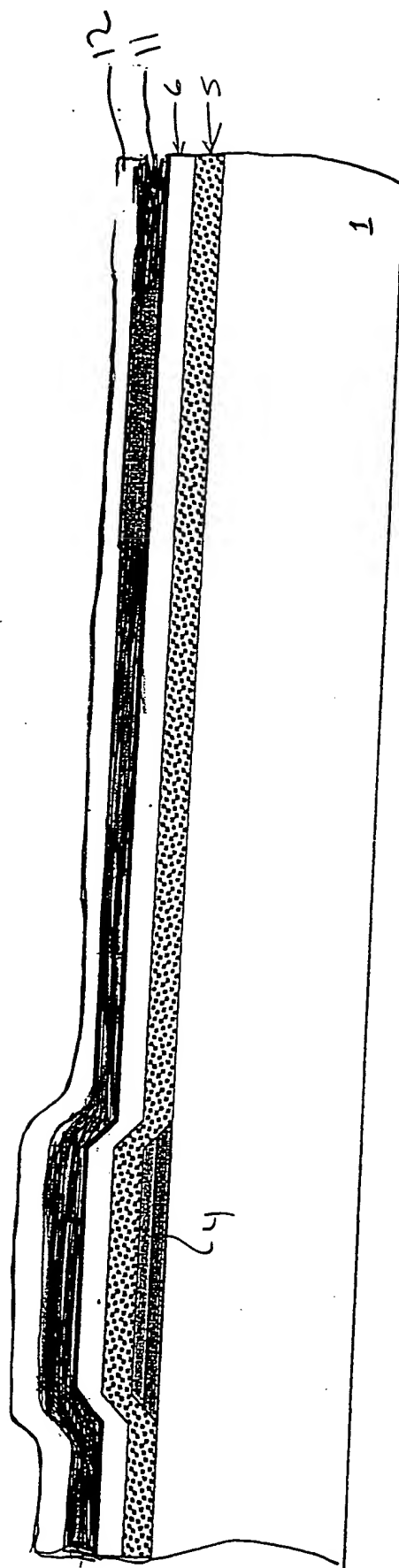


FIG. 8B

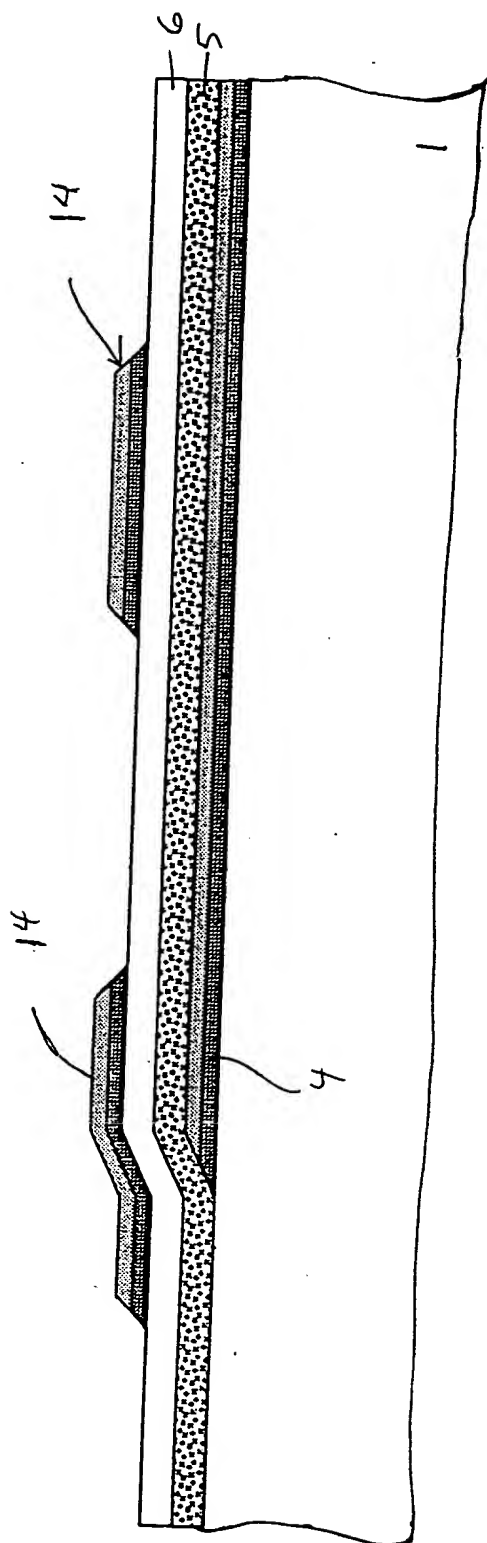


FIG. 9A

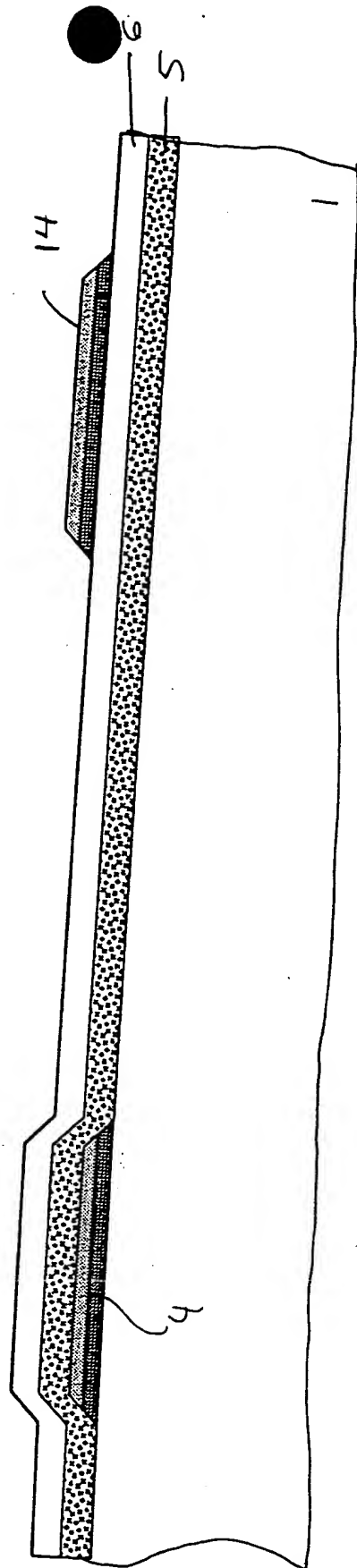


FIG. 9B

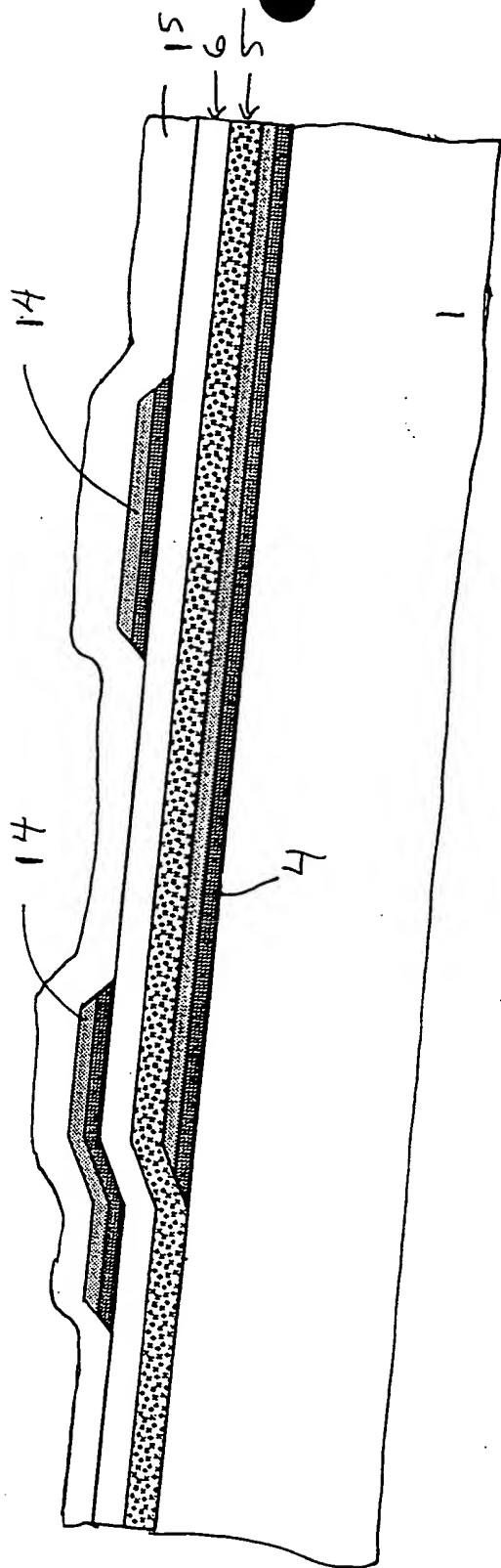


FIG. 10A

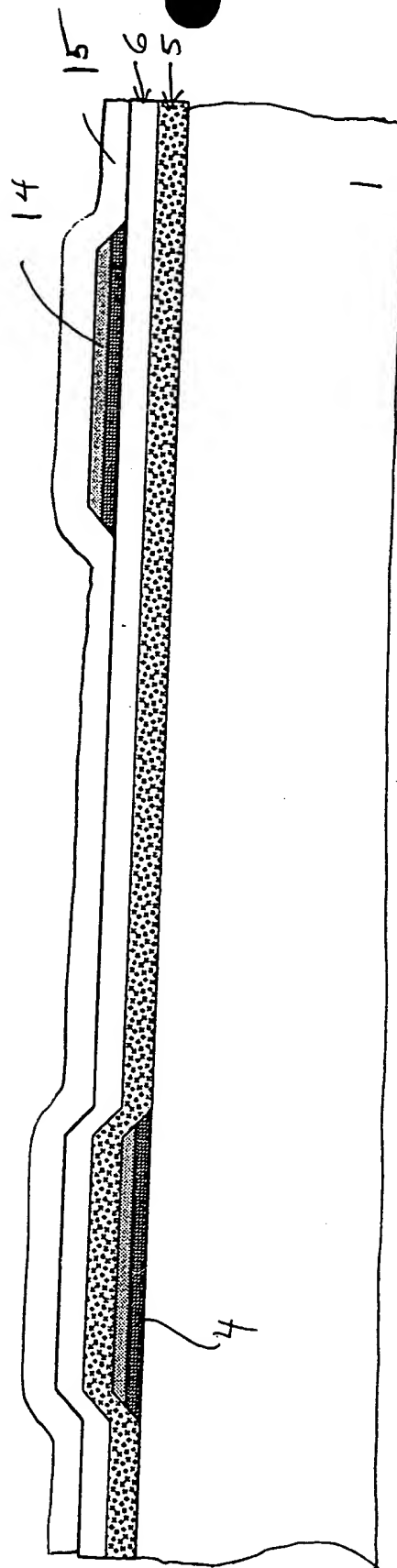


FIG. 10B

FIG. 11A

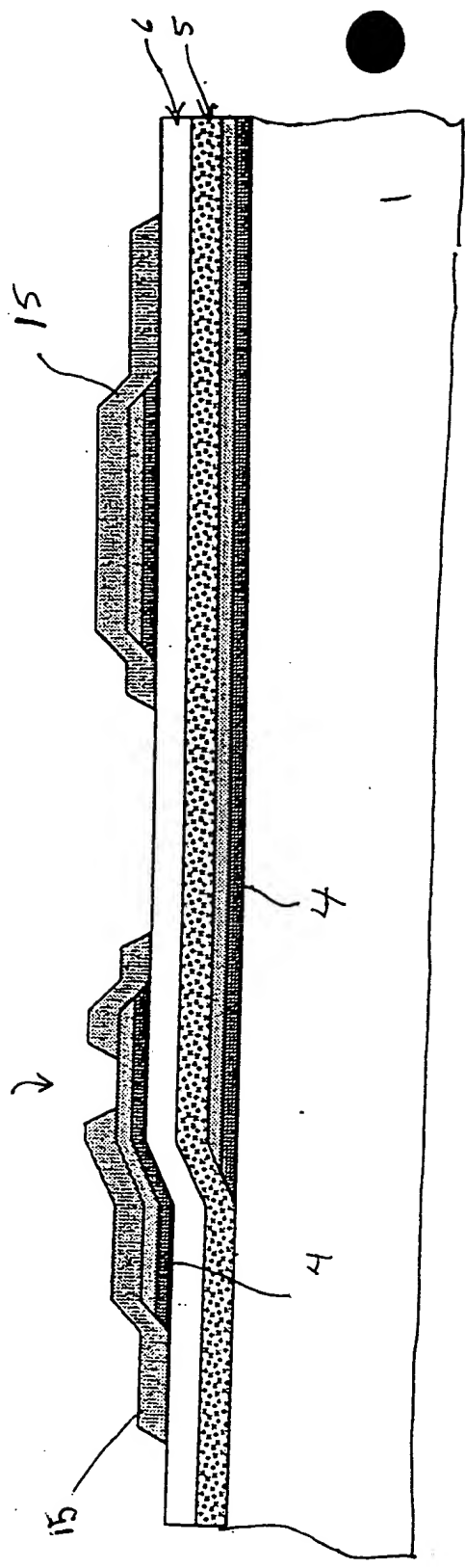


FIG. 11A

FIG. 11B

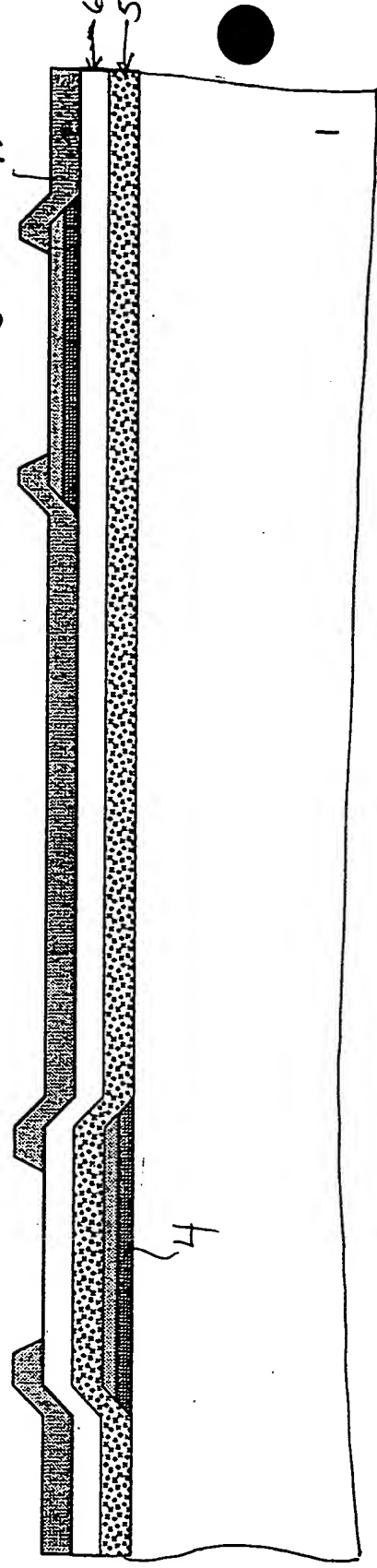


FIG. 11B

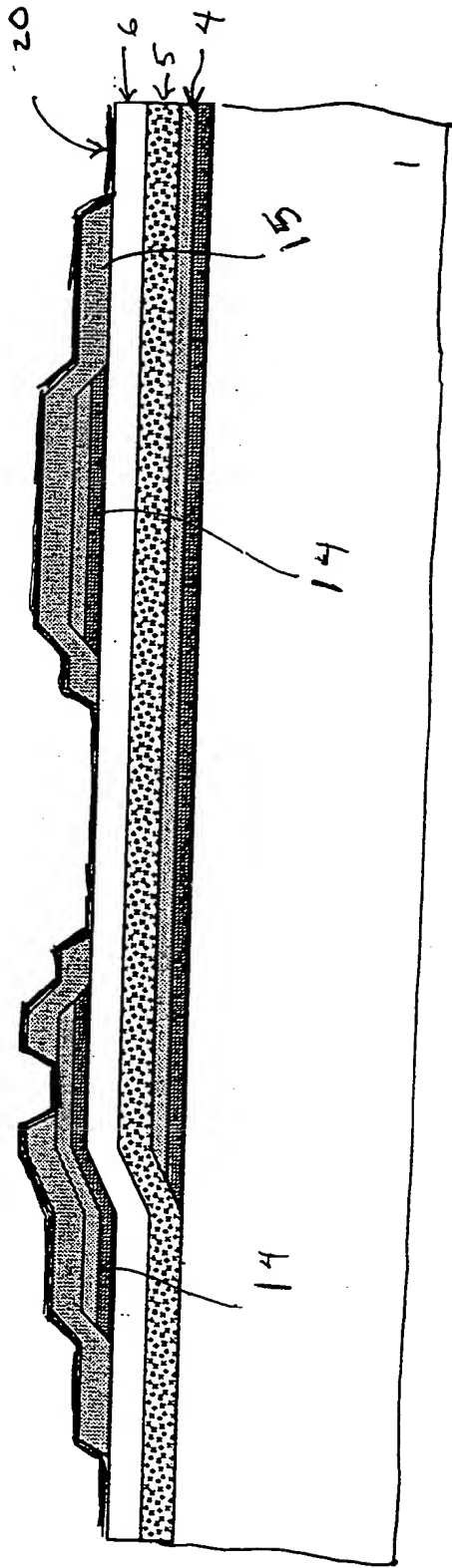


FIG. 12A

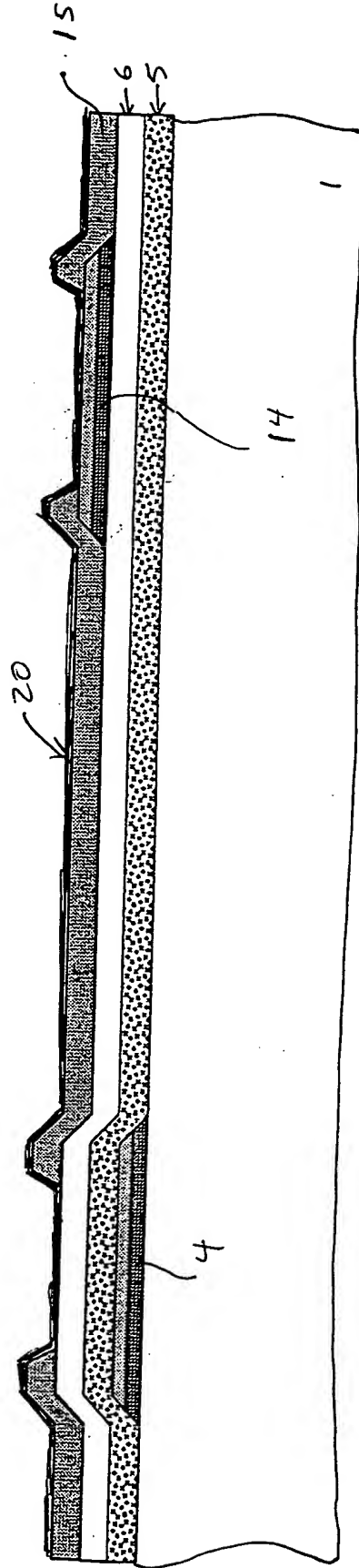


FIG. 12B

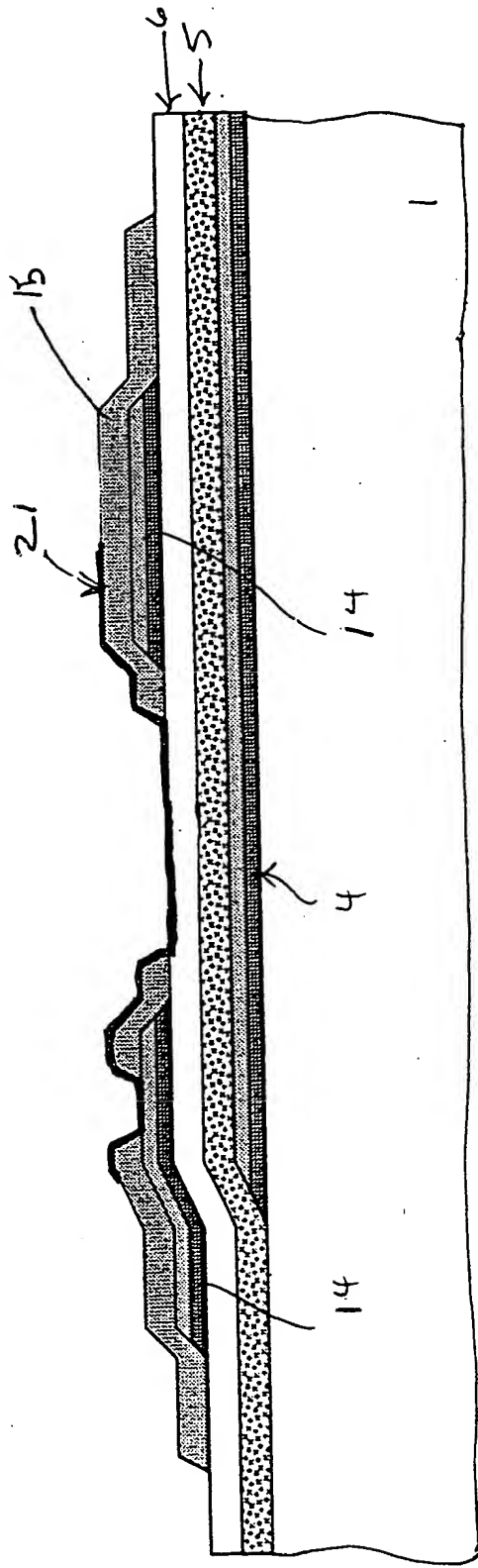


FIG. 13A

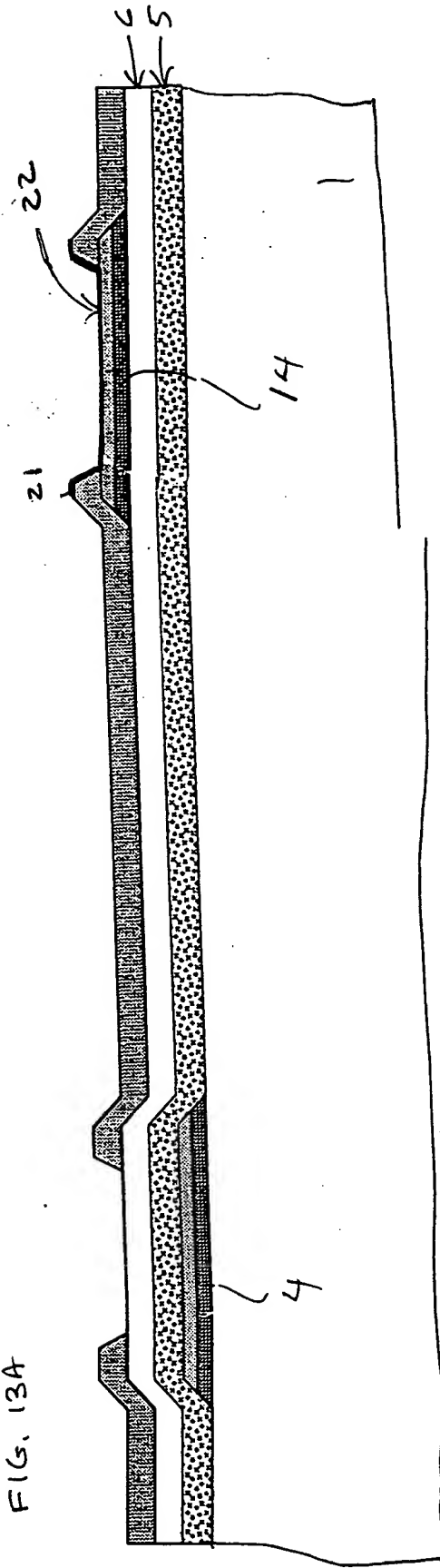


FIG. 13B

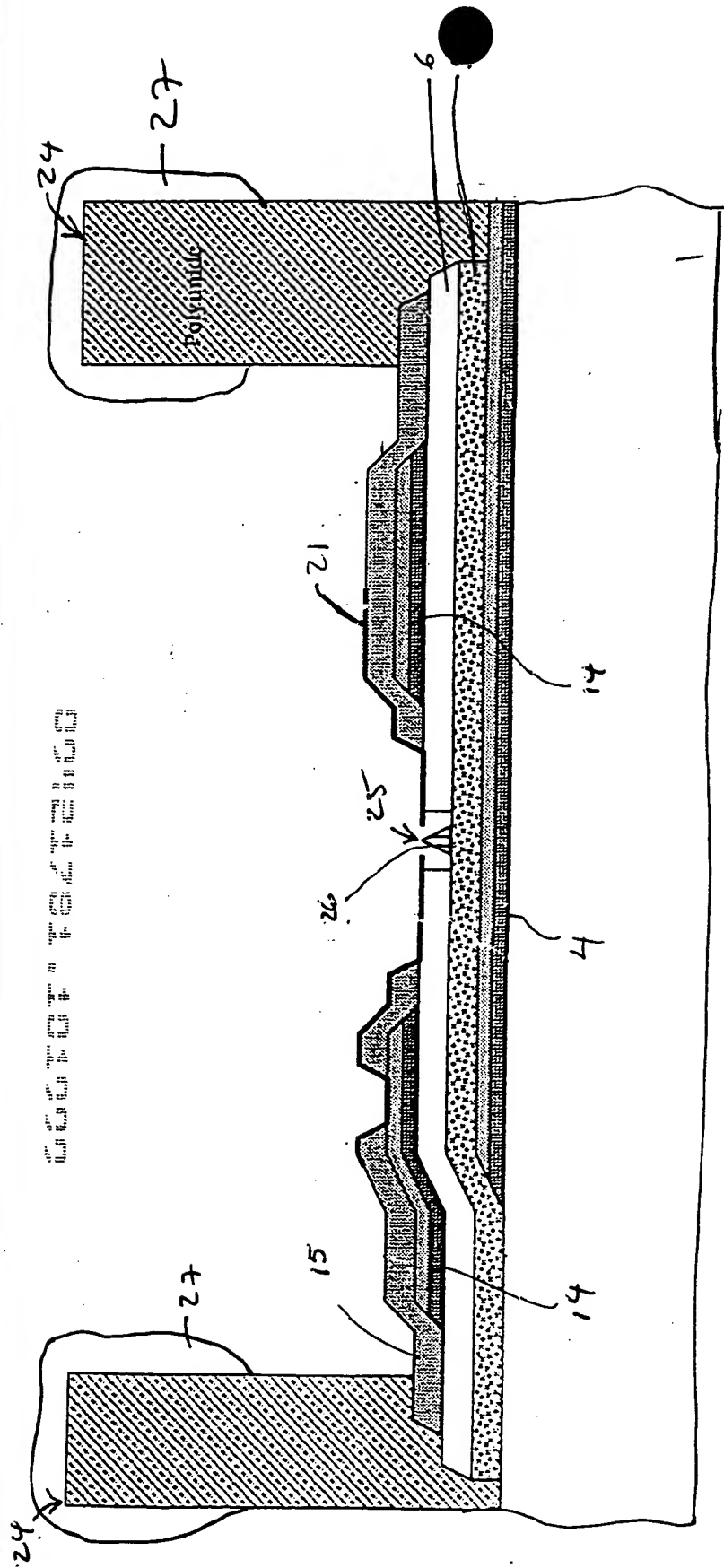


FIG. 14A

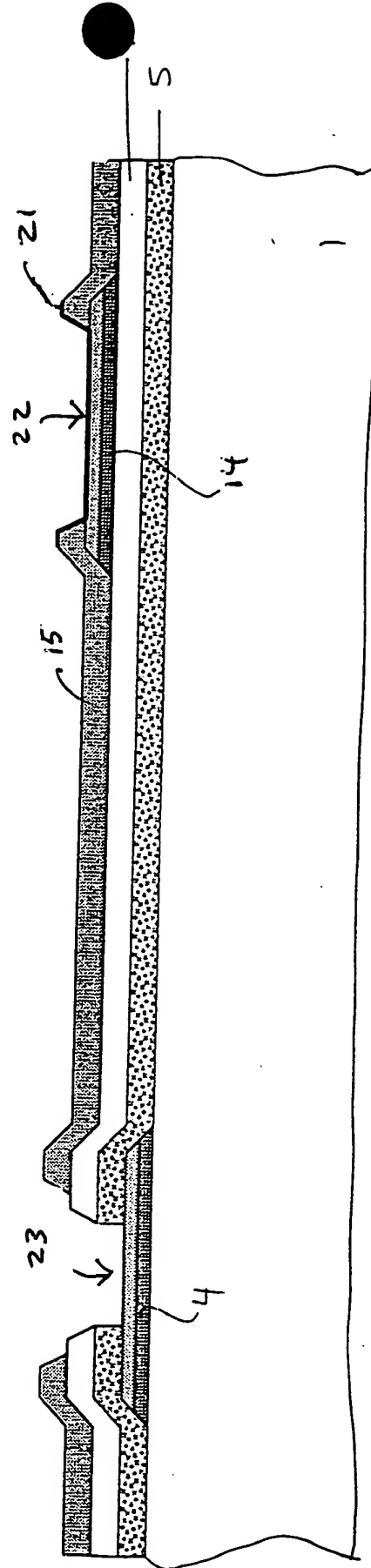


FIG. 14B

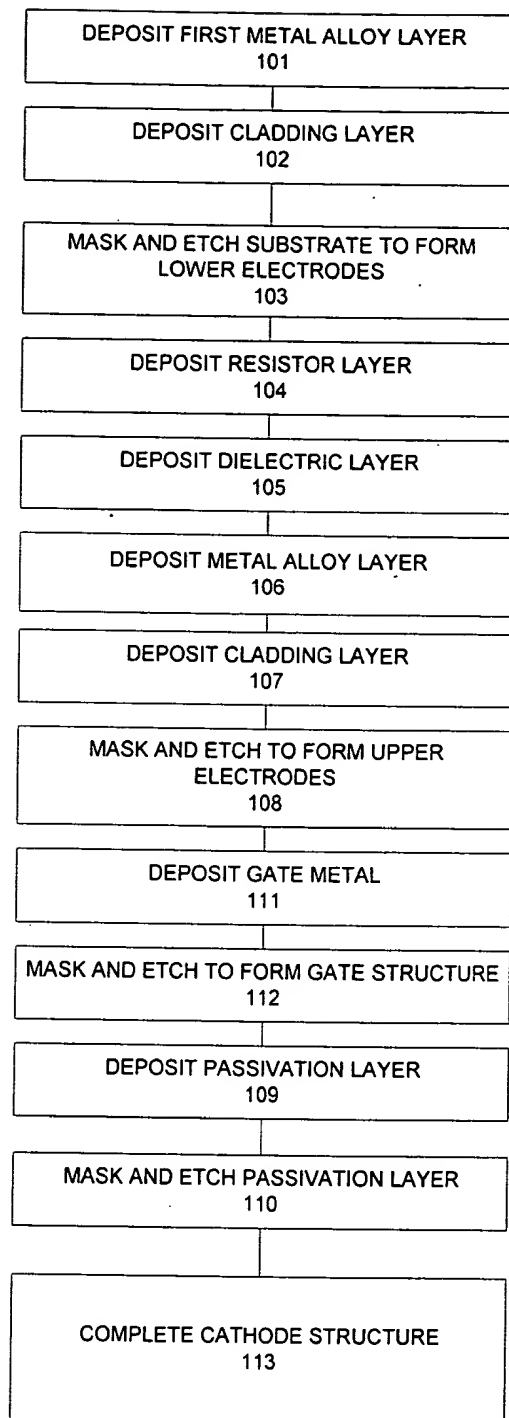


FIG. 15

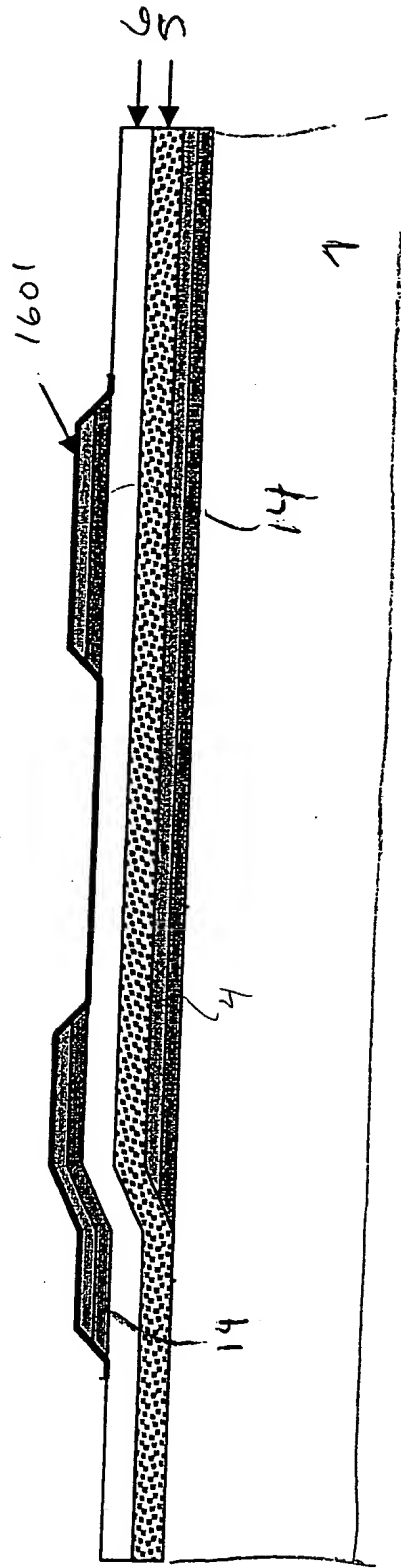


FIG. 16A

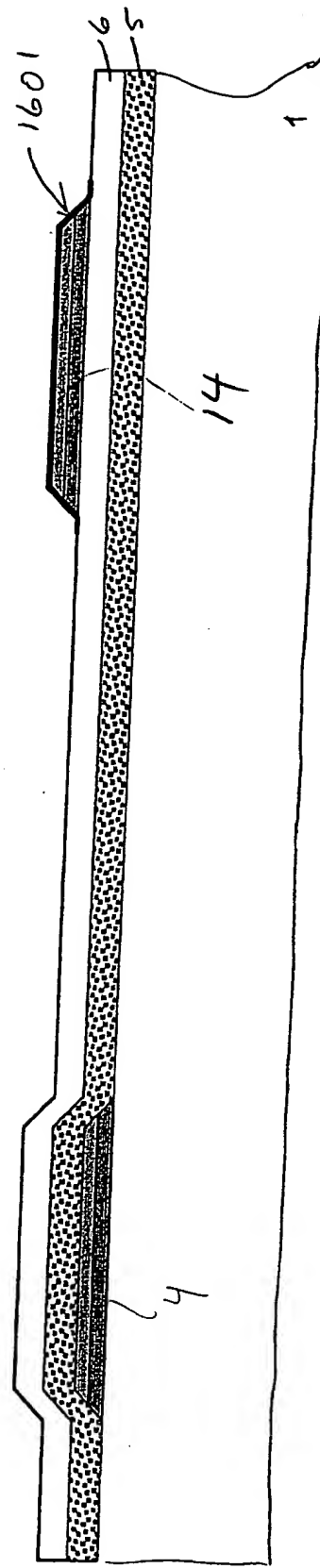


FIG. 16B

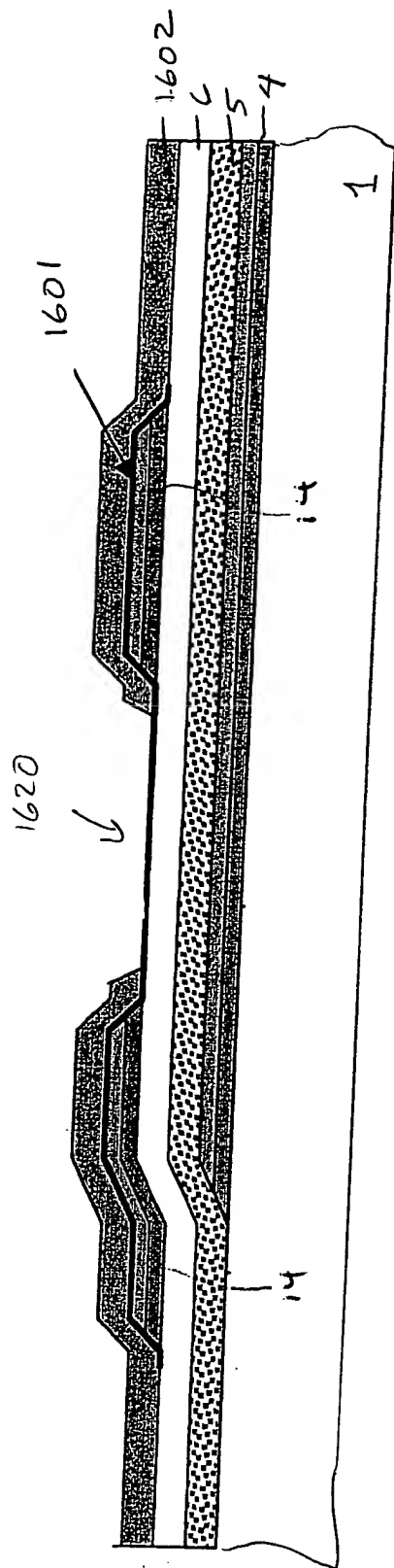


FIG. 16C

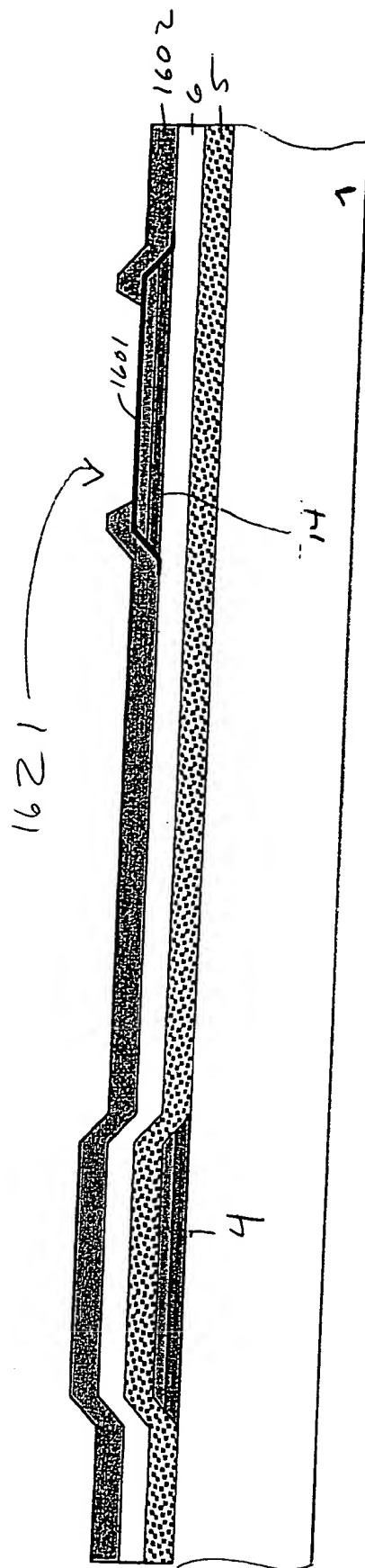
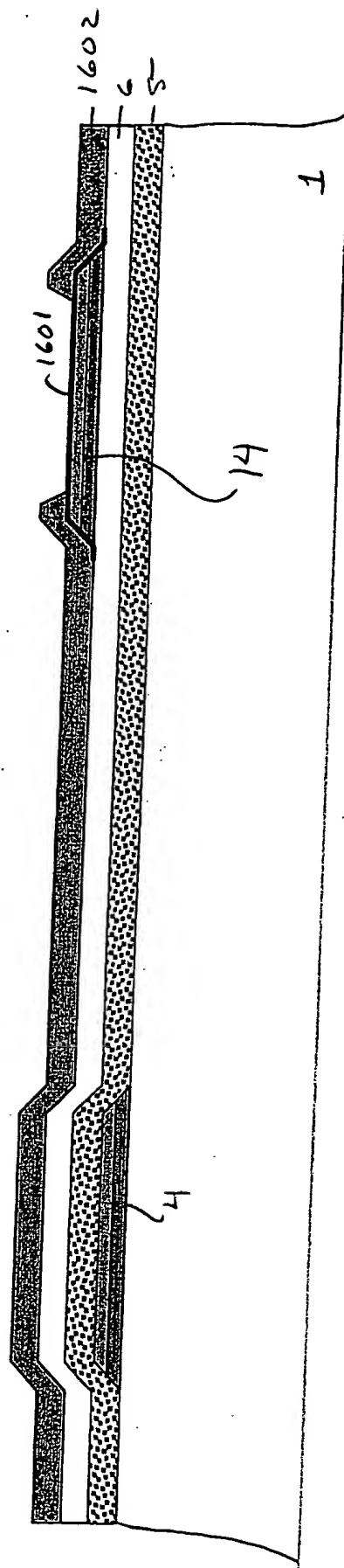
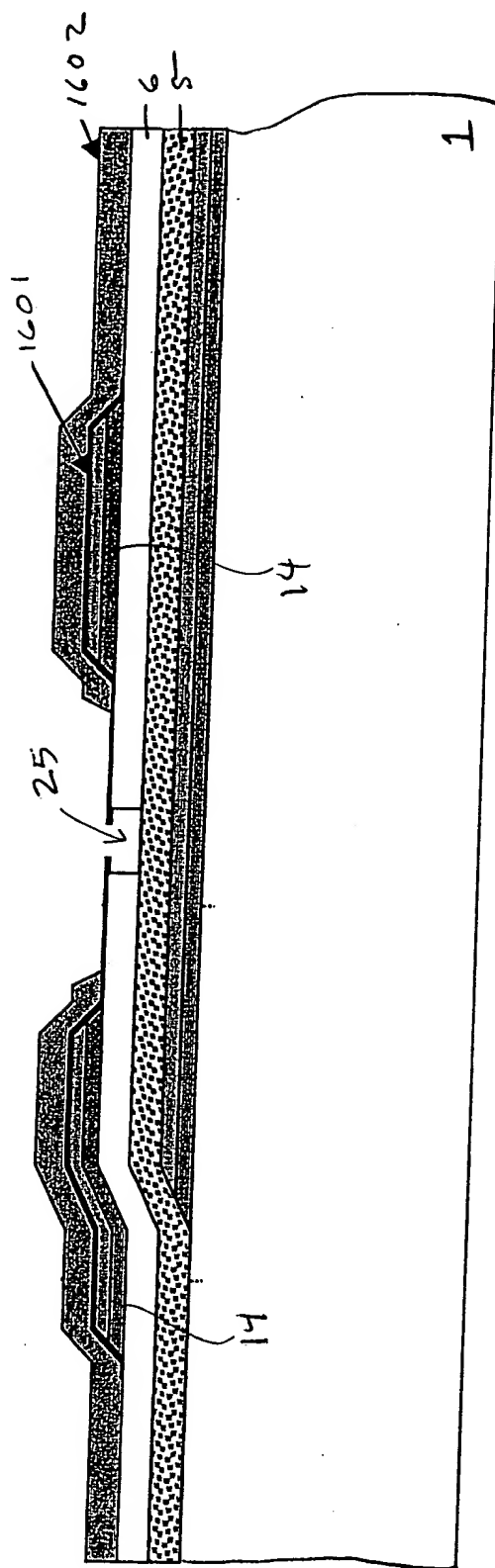


FIG. 16D



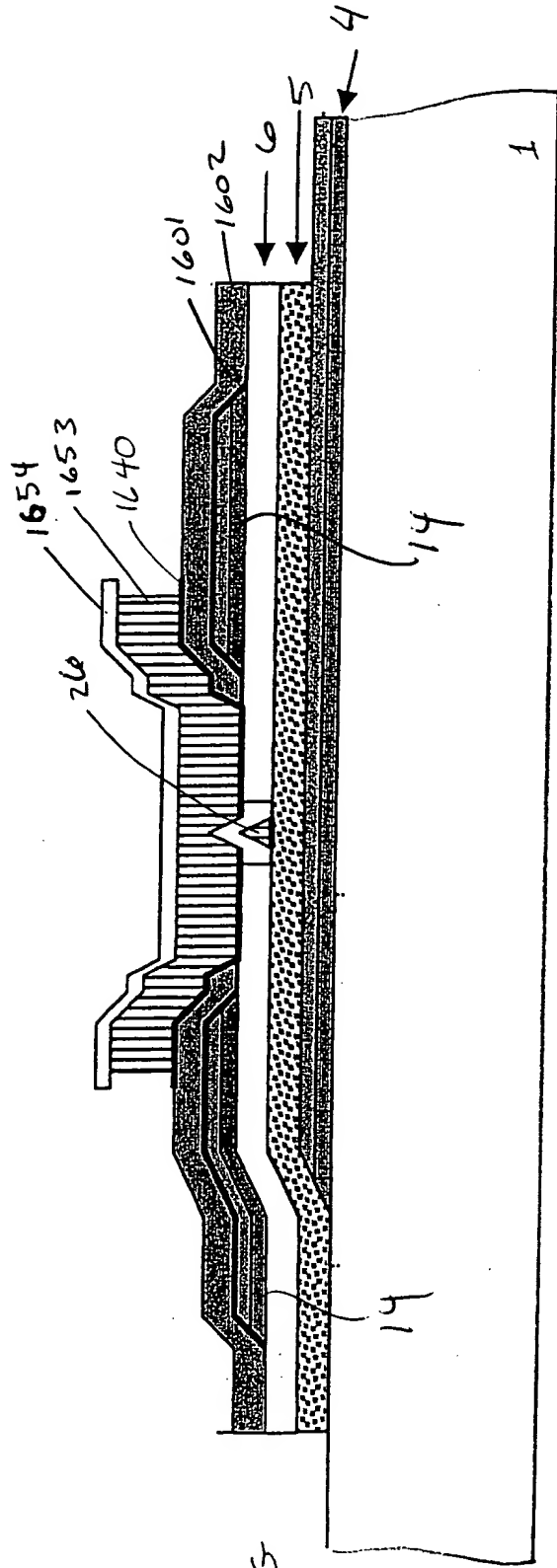


FIG 16G

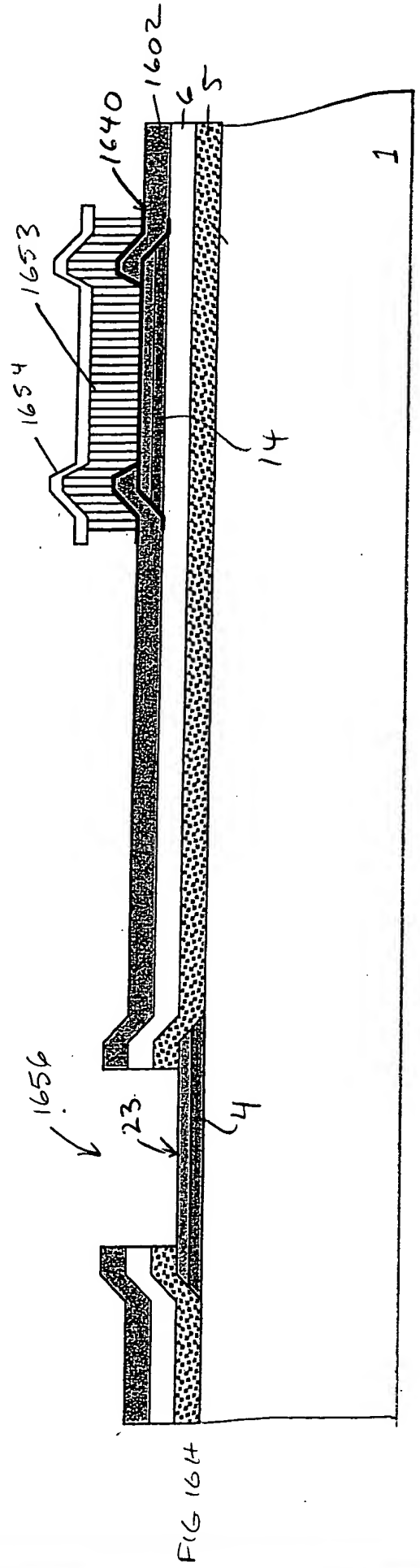


FIG 16H

FIG. 16 I

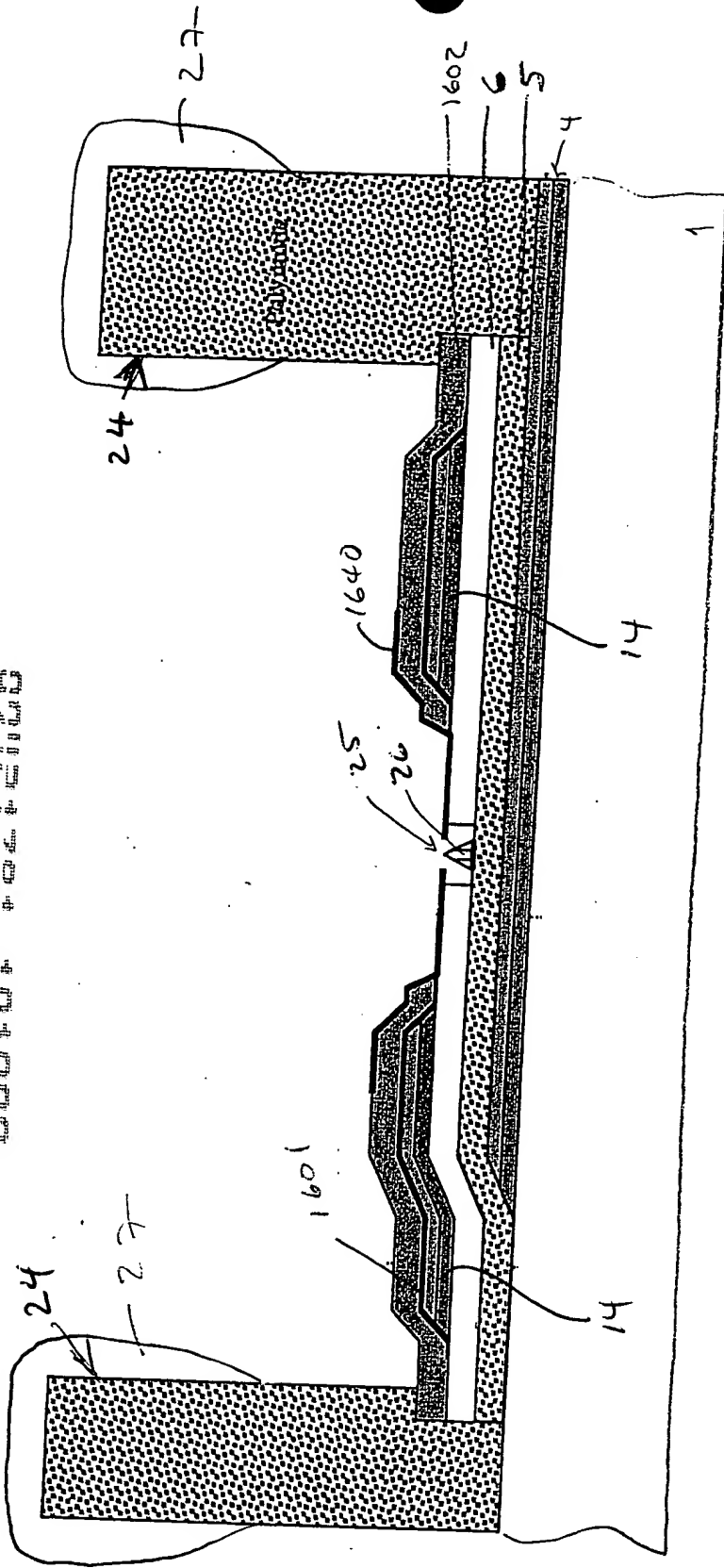


FIG 16 I

1656

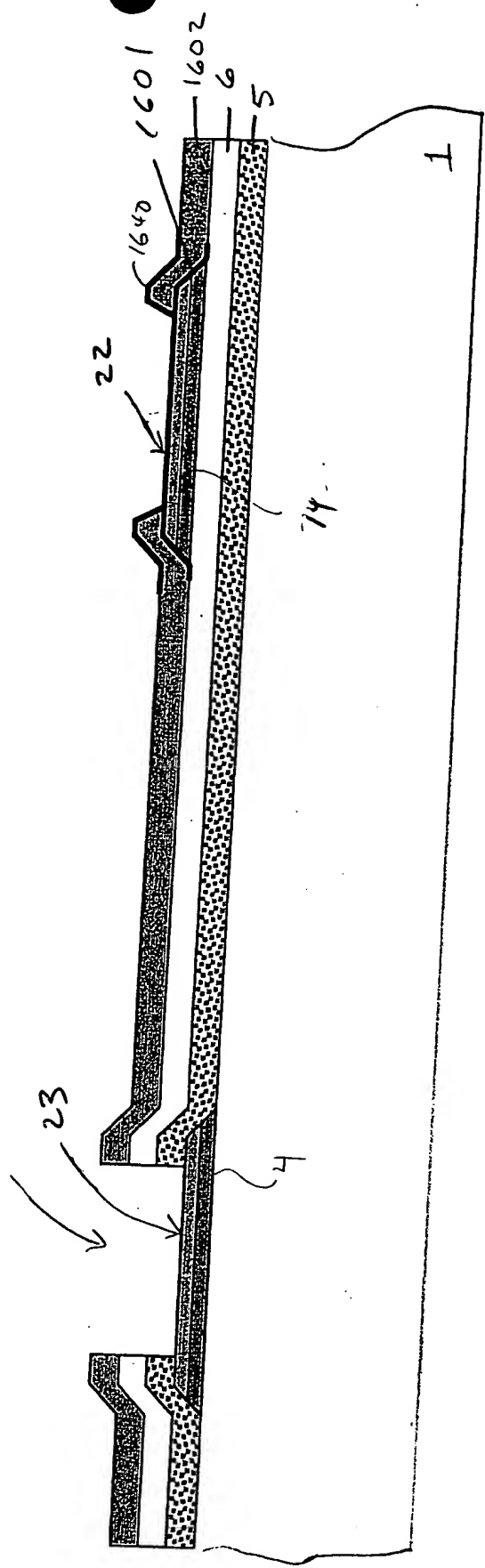


FIG 16 J

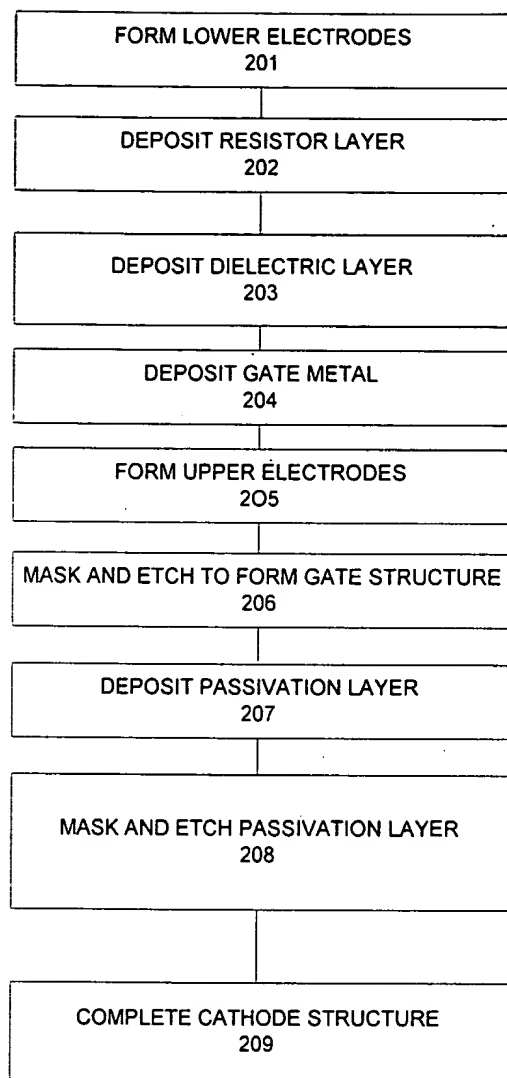
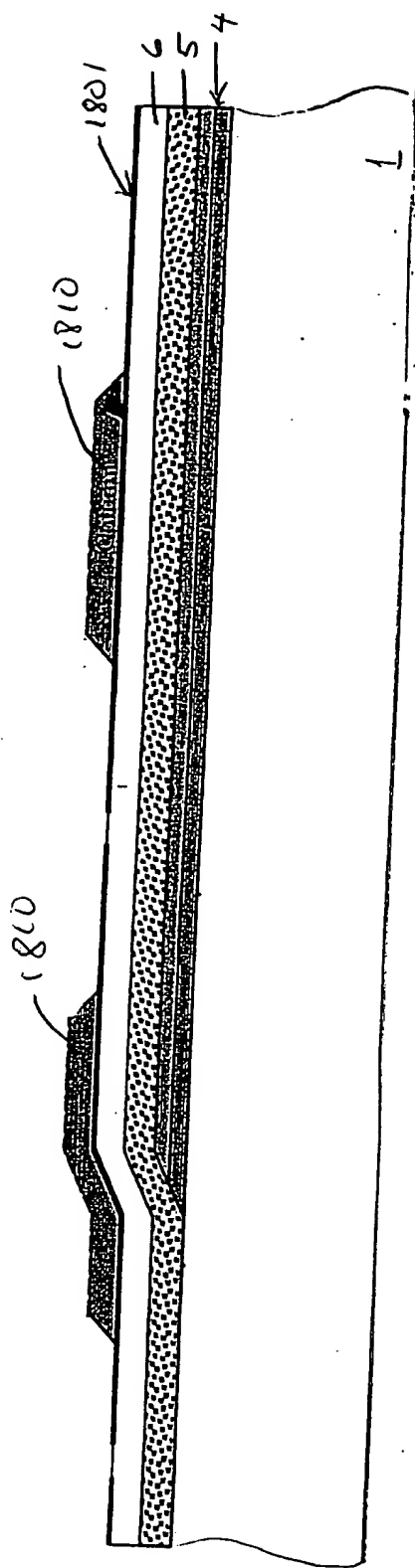


FIG. 17

[illegible]

41518A

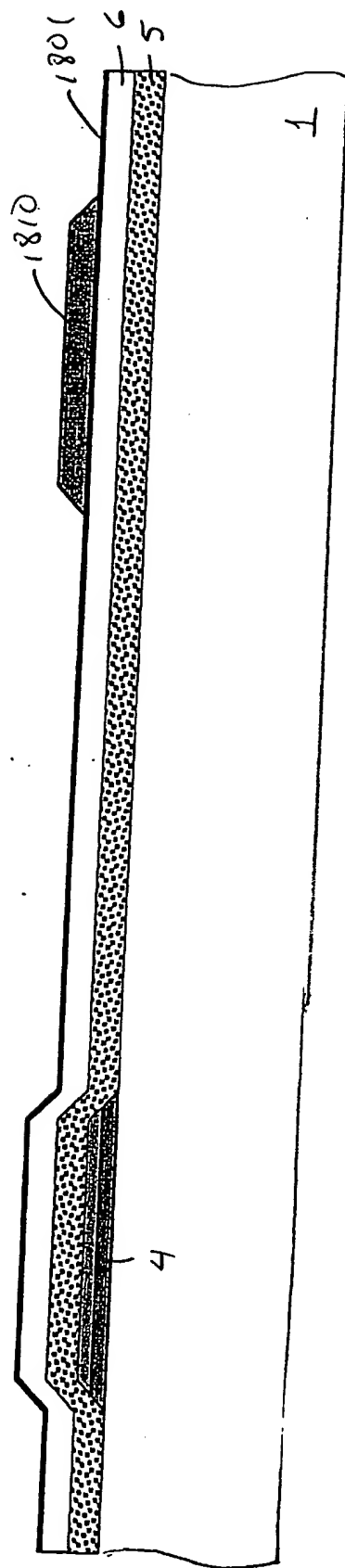
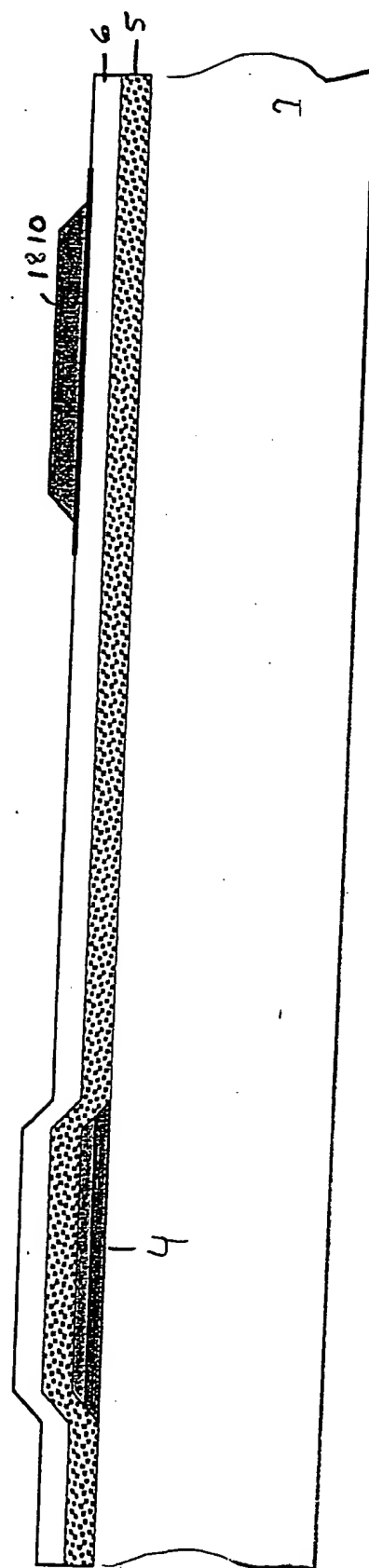
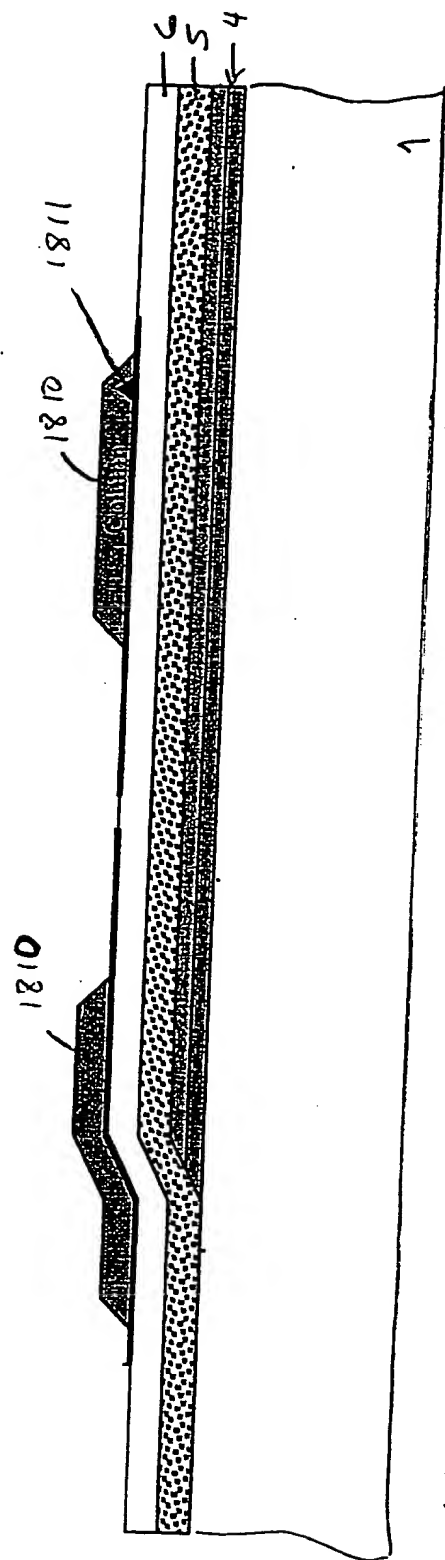
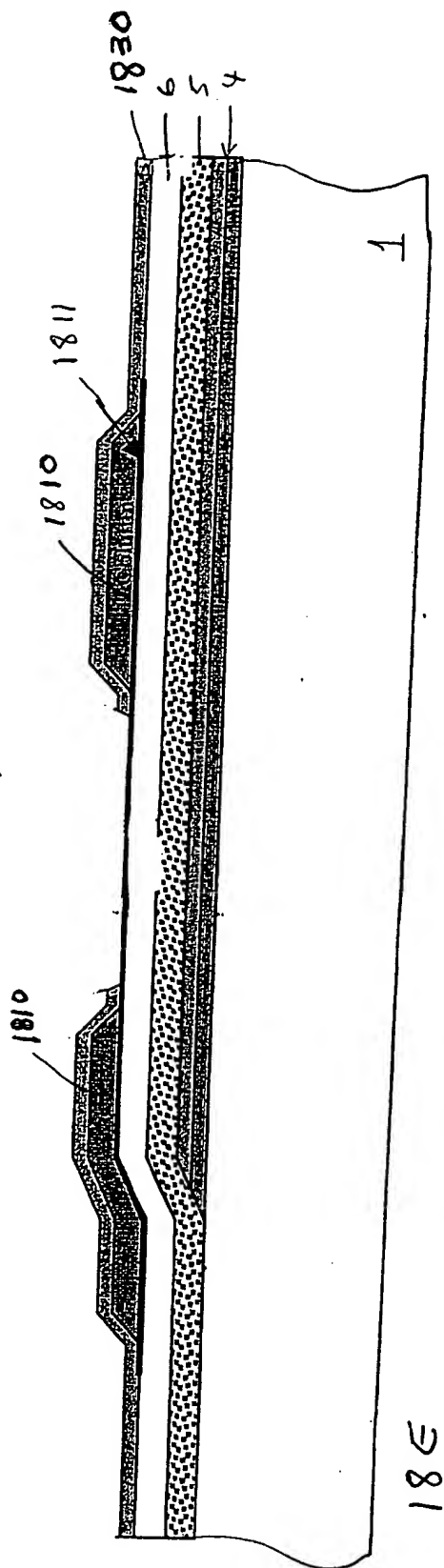


Fig. 18B



1820



1820

1281

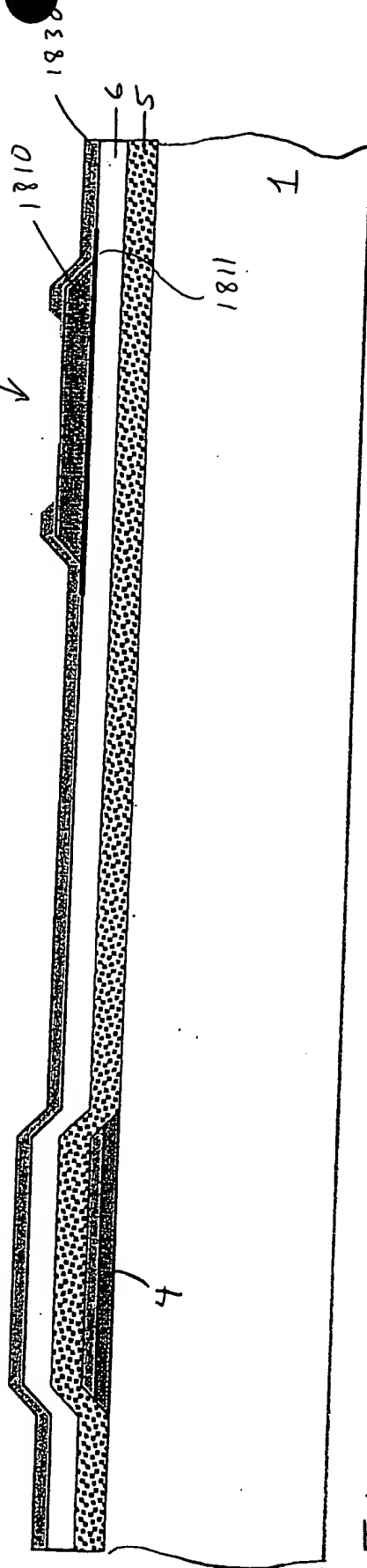


FIG. 18F

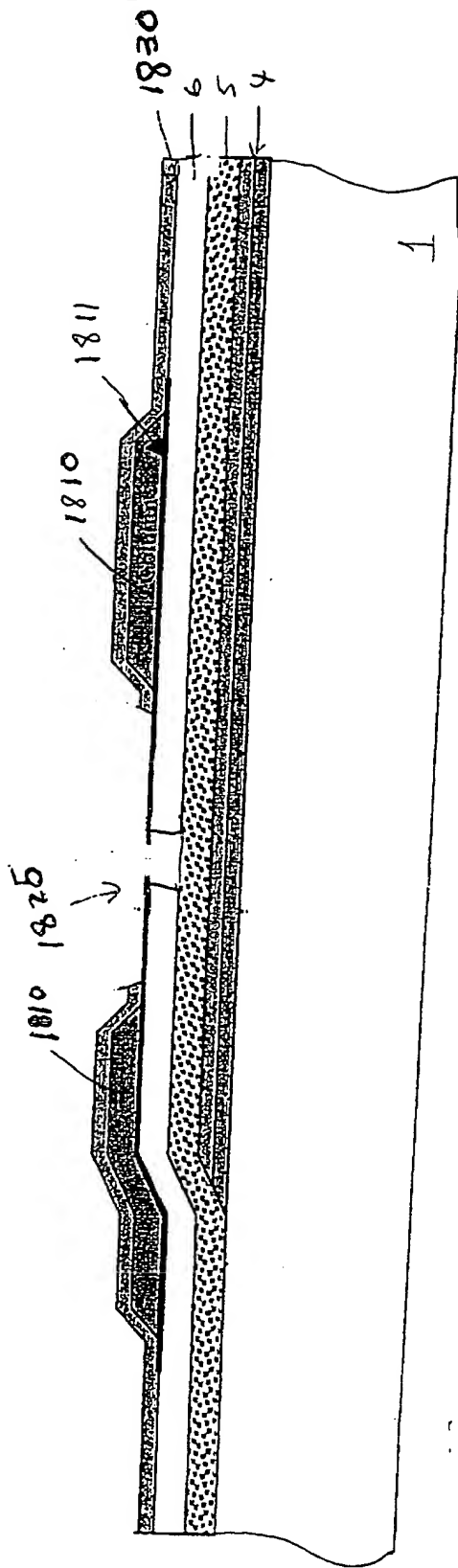


FIG. 18G

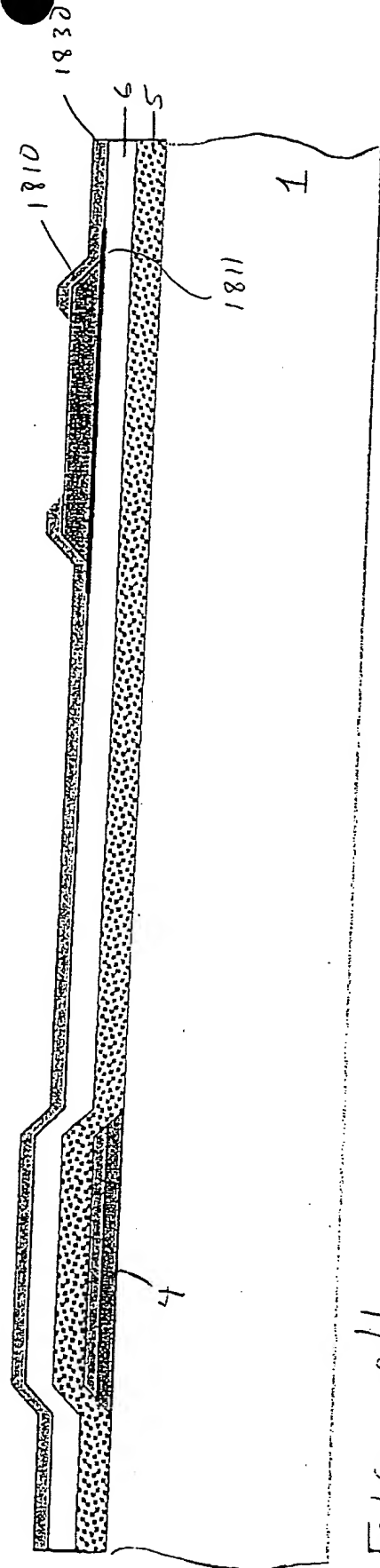


FIG. 18H

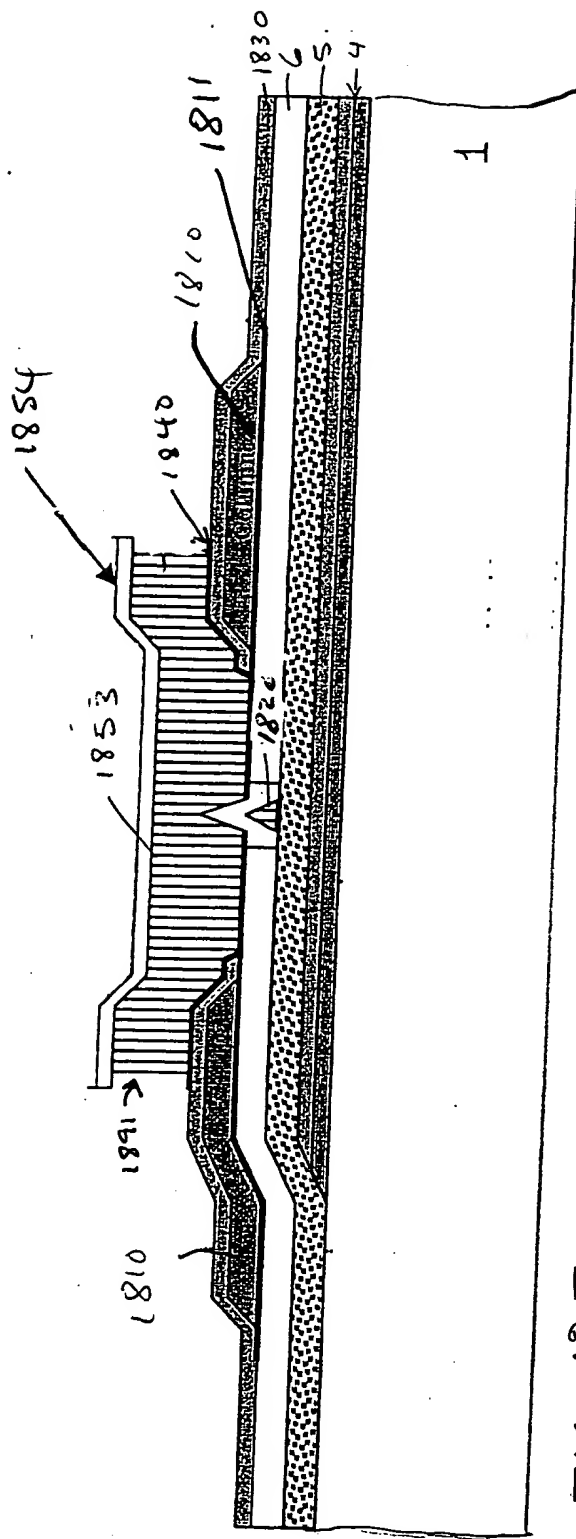


FIG 18 I

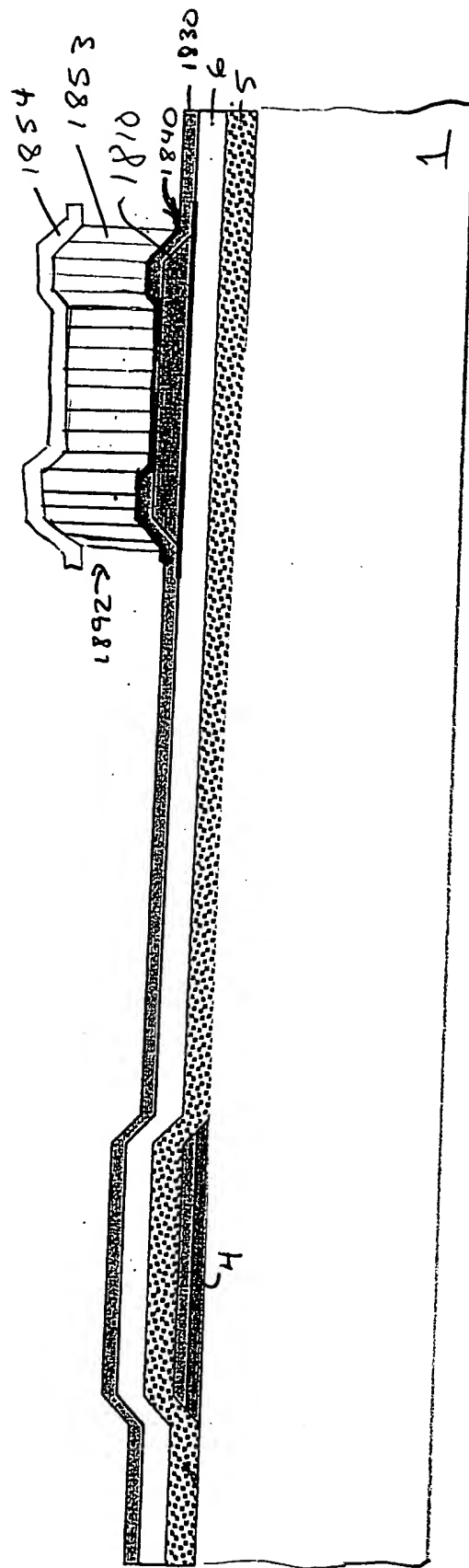


FIG 18 J

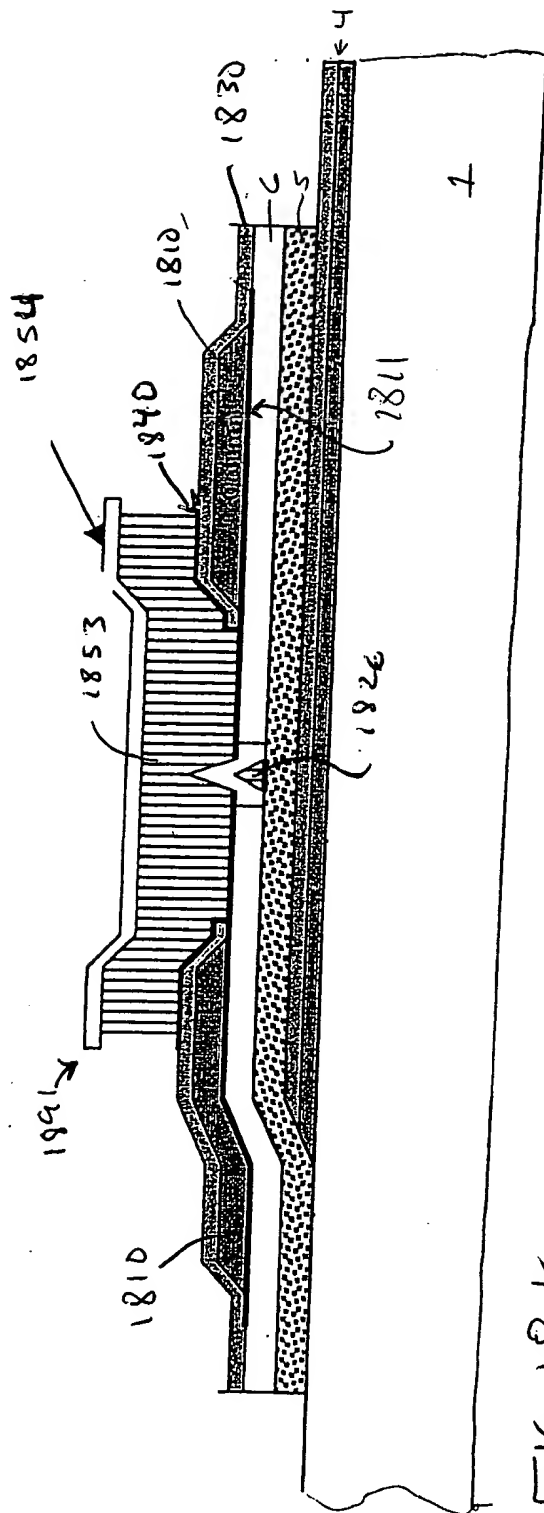


FIG 18 K

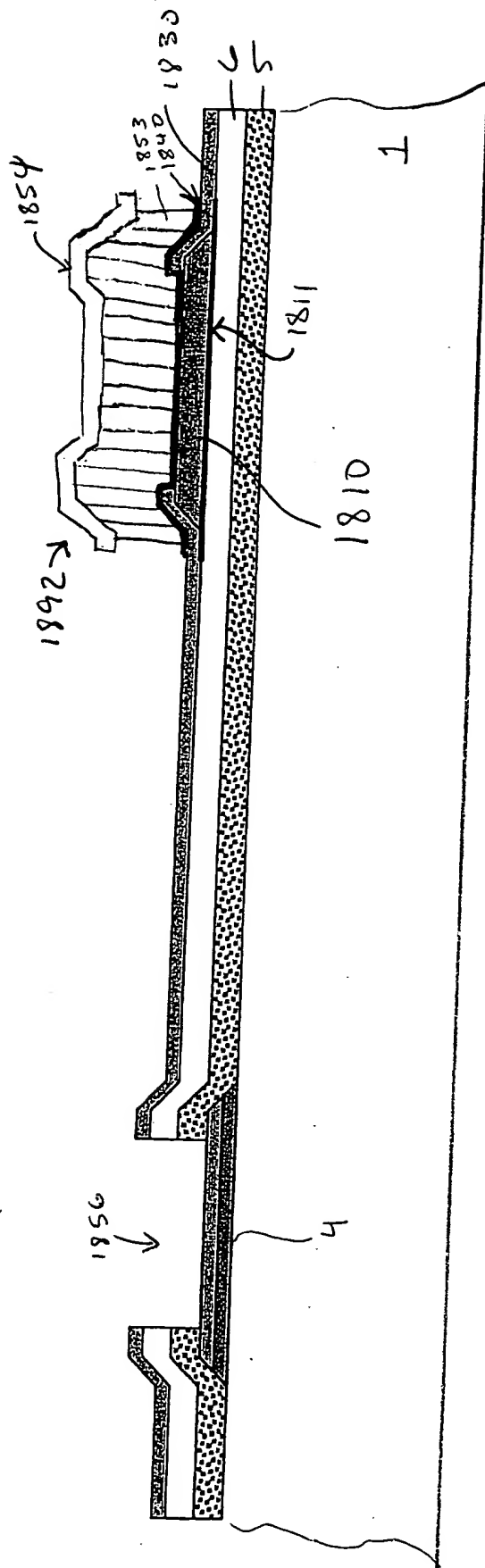


FIG 18 L

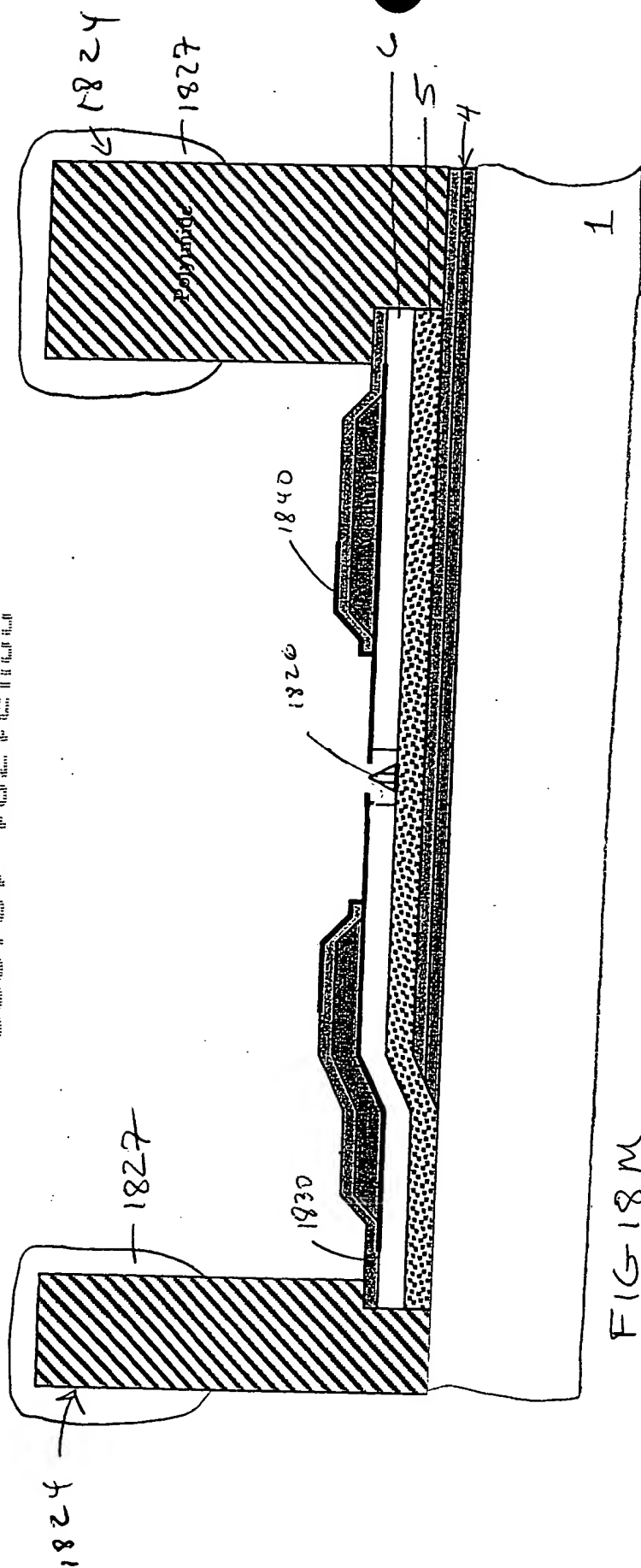
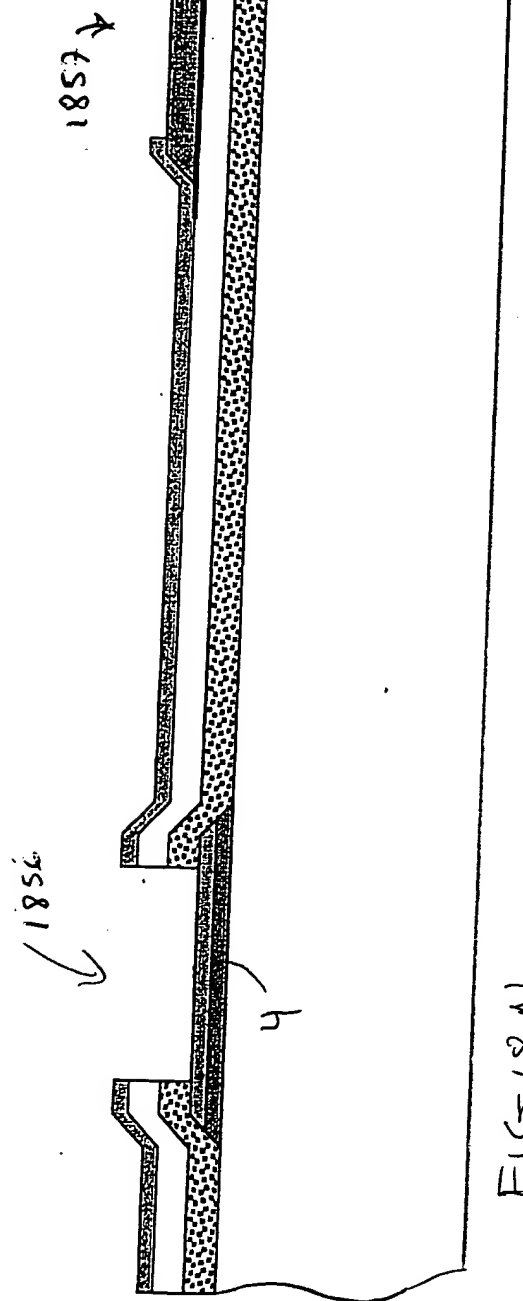


FIG-18M



4151822

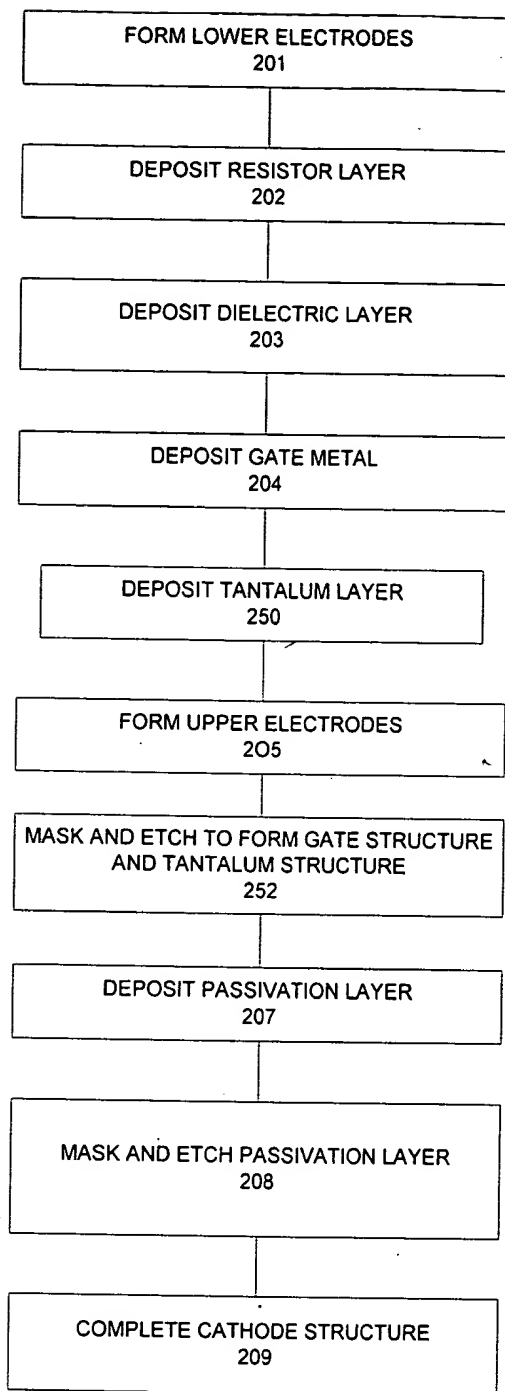


FIG. 19

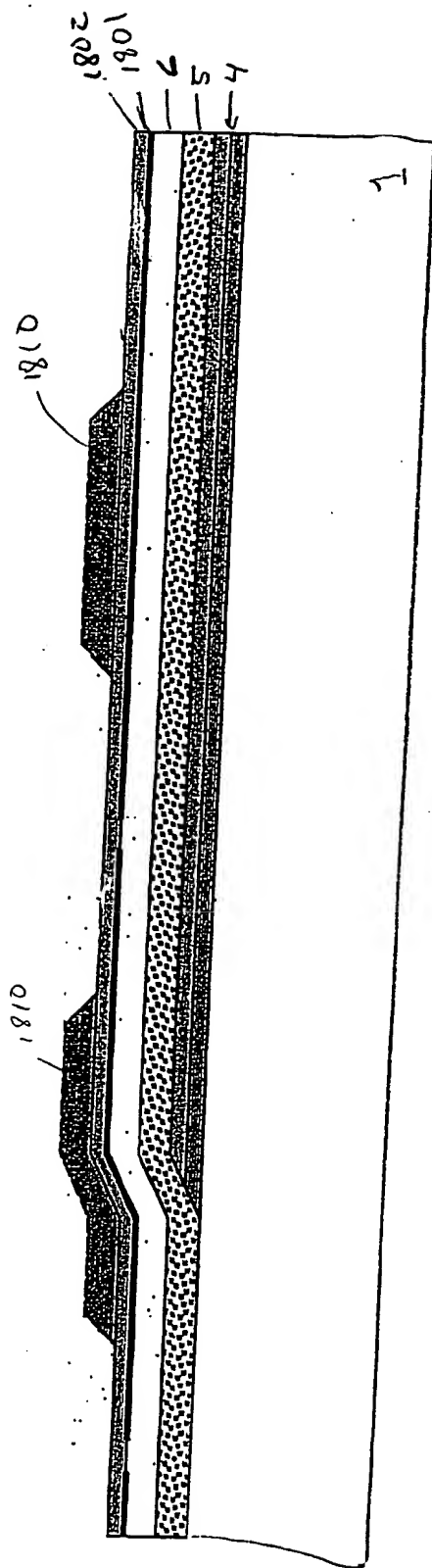


FIG. 20A

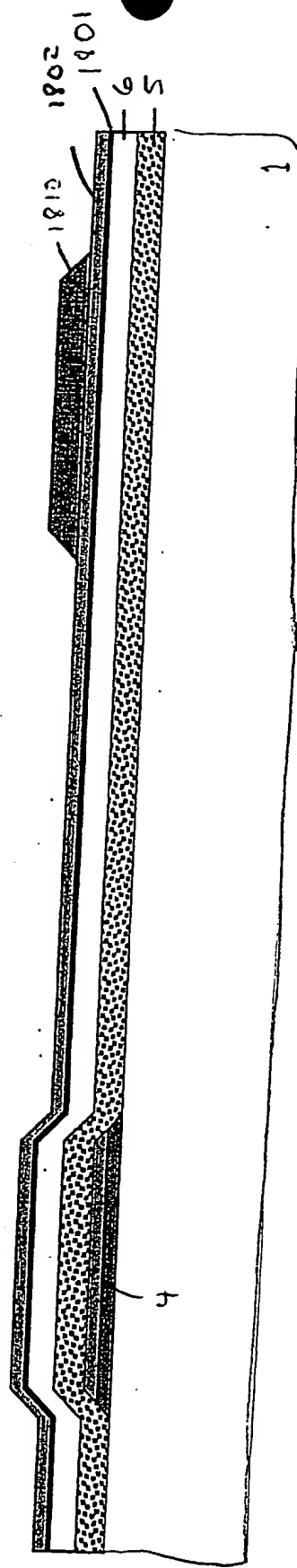
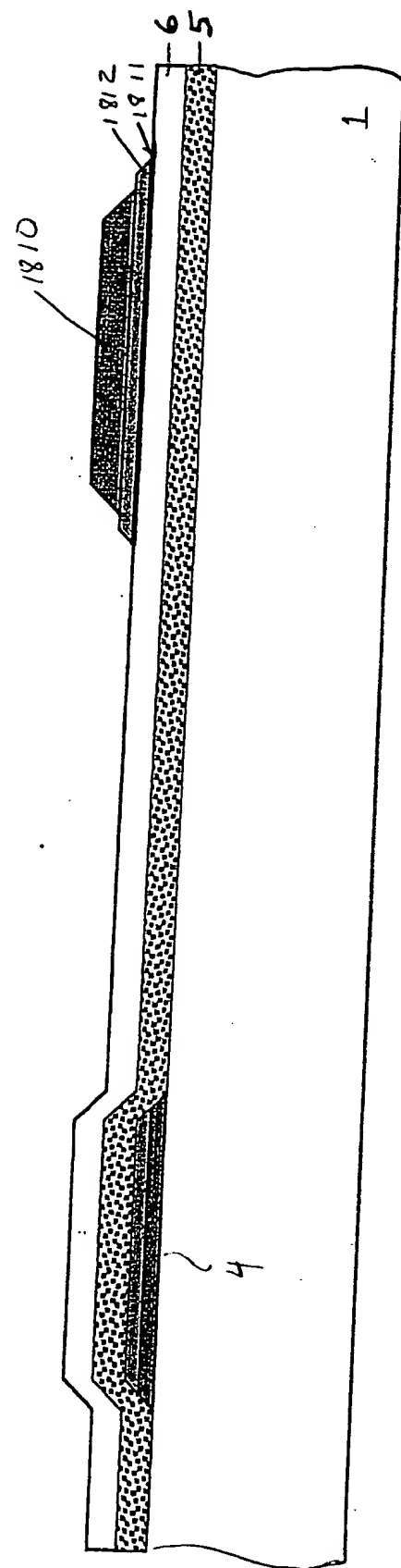
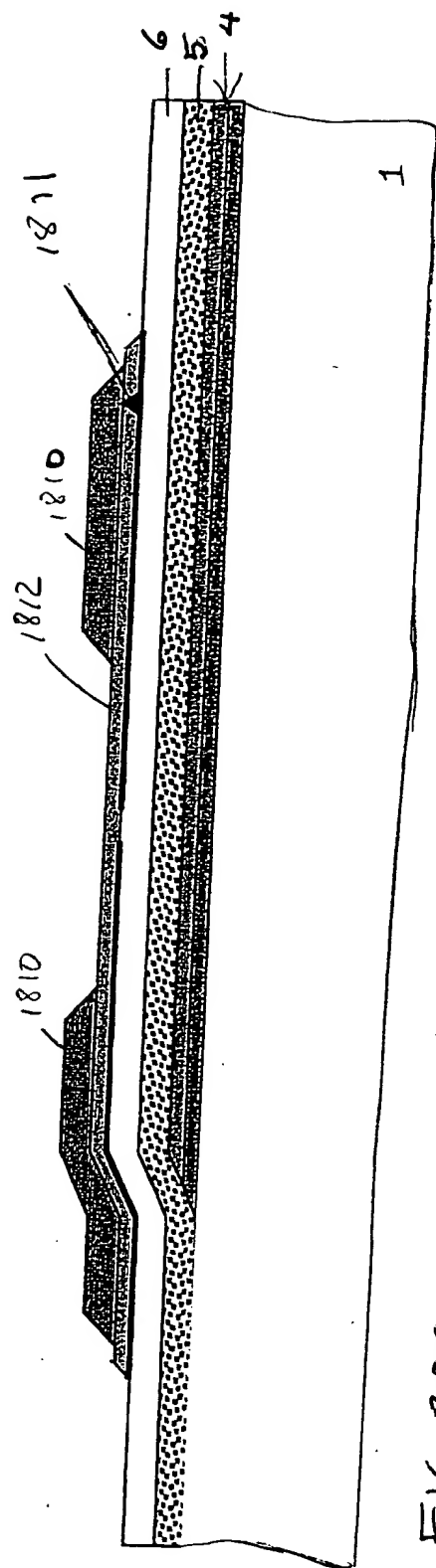


FIG. 20B



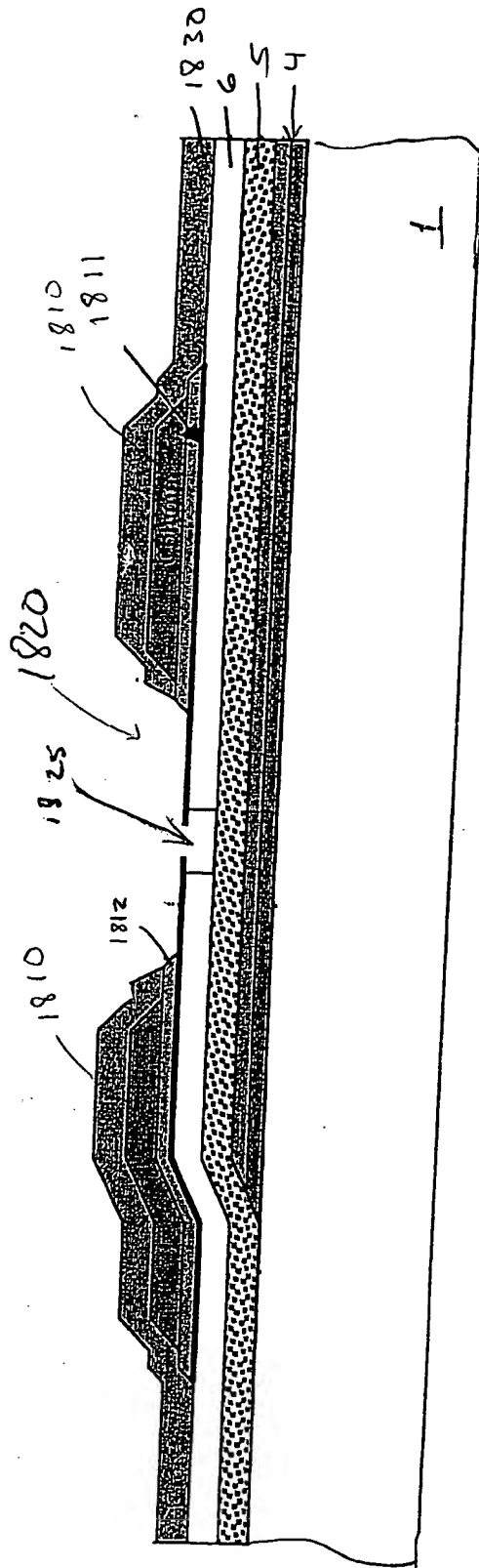


FIG 20E

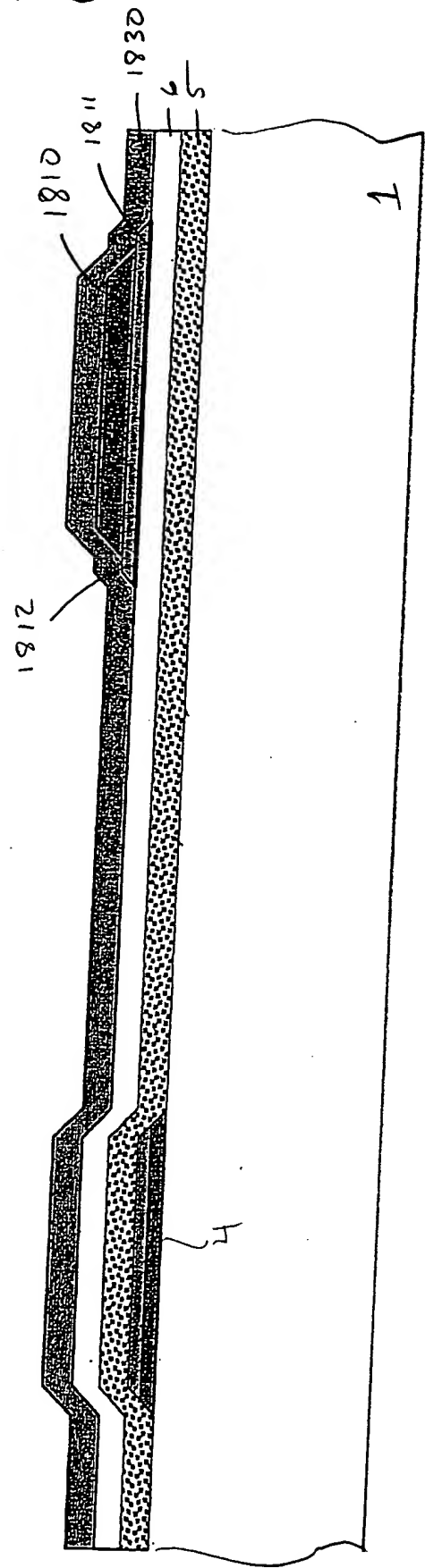


FIG 20F

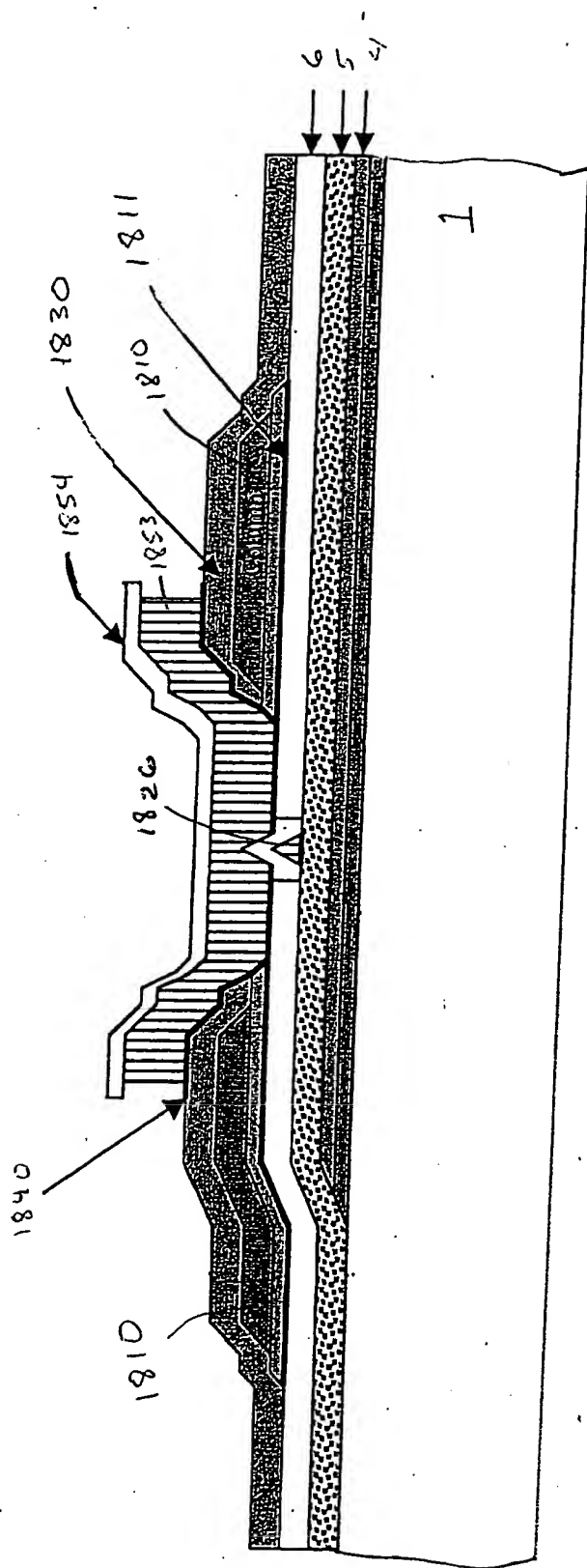


FIG. 20G

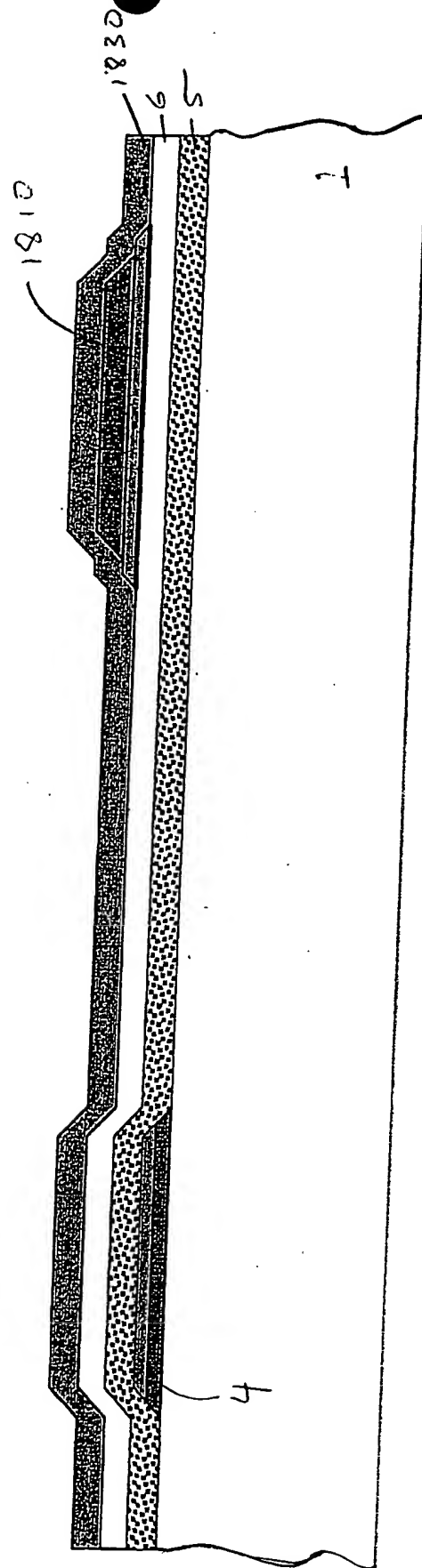


FIG. 20H

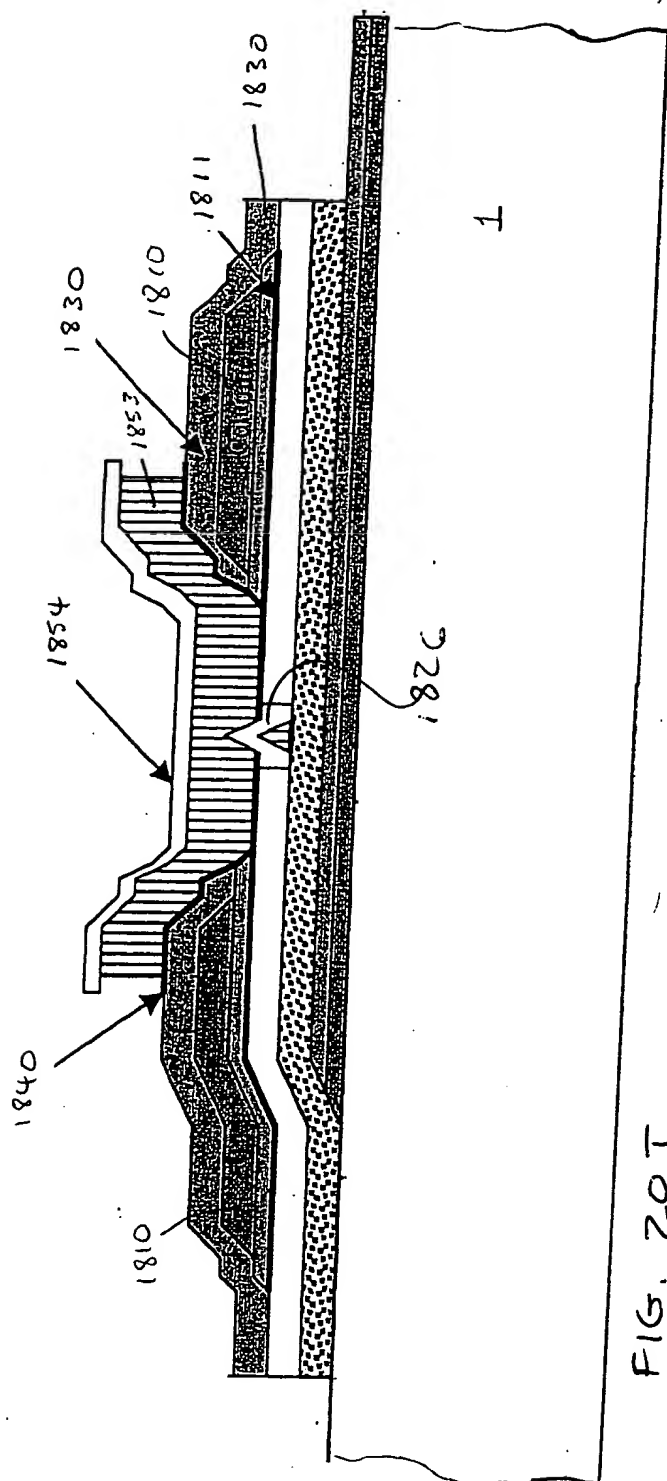


FIG. 20H

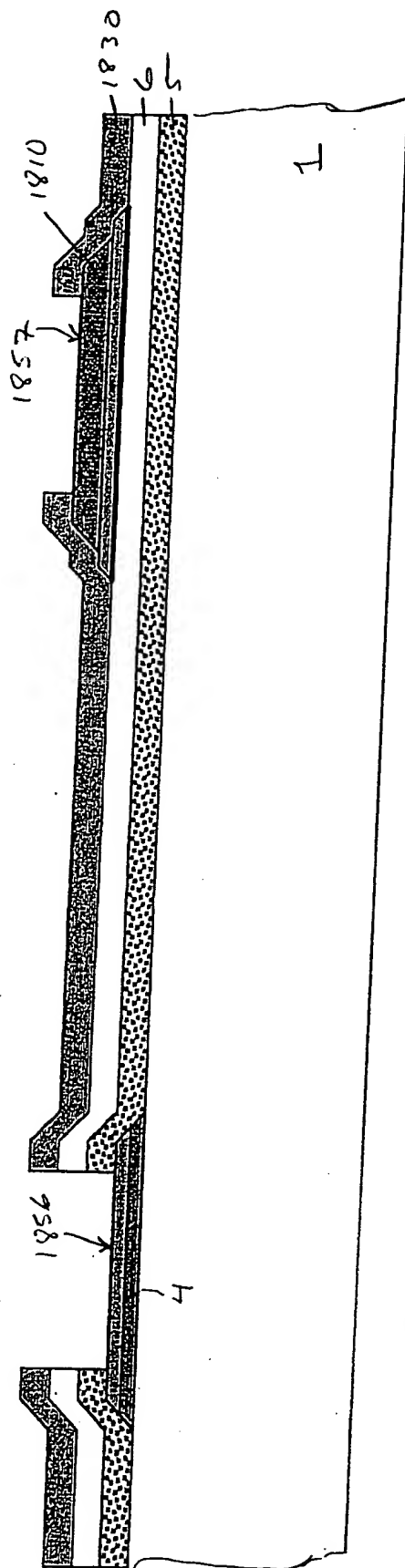


Fig. 20.5

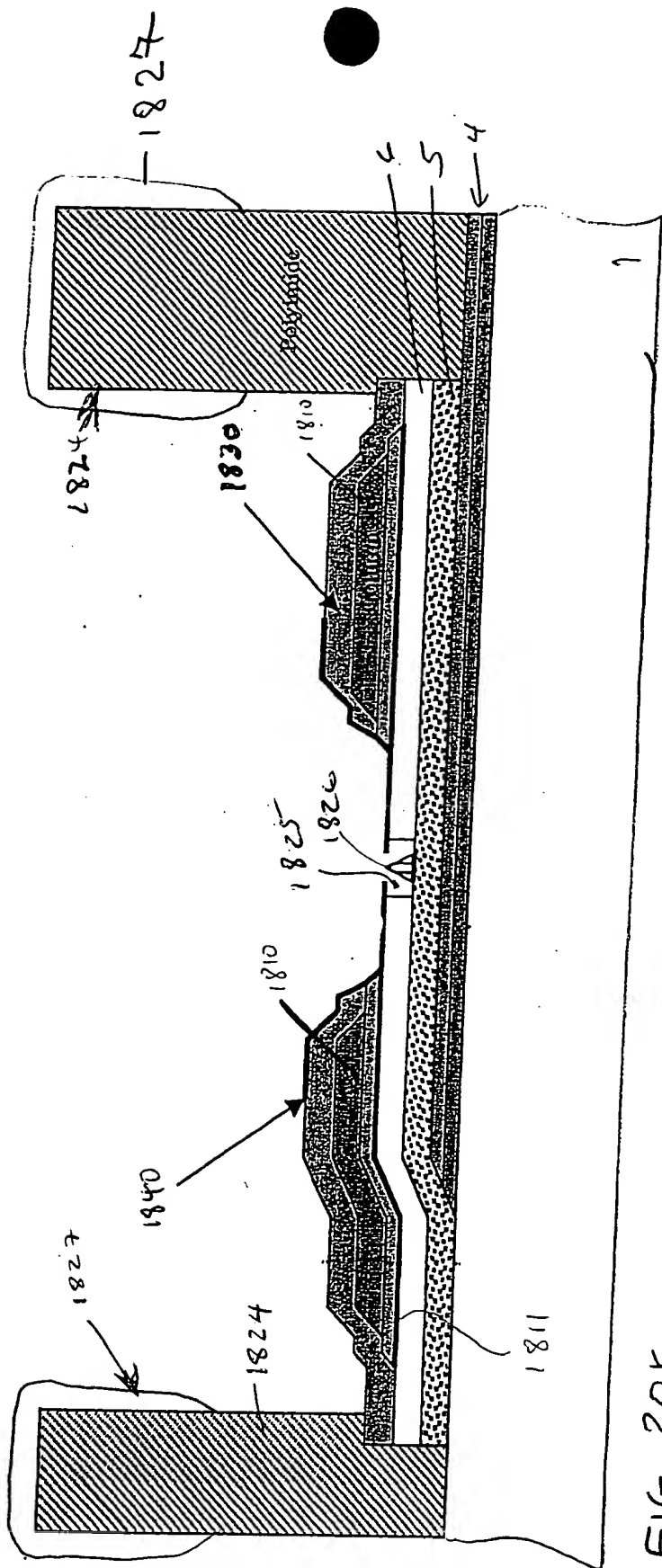


FIG 20K

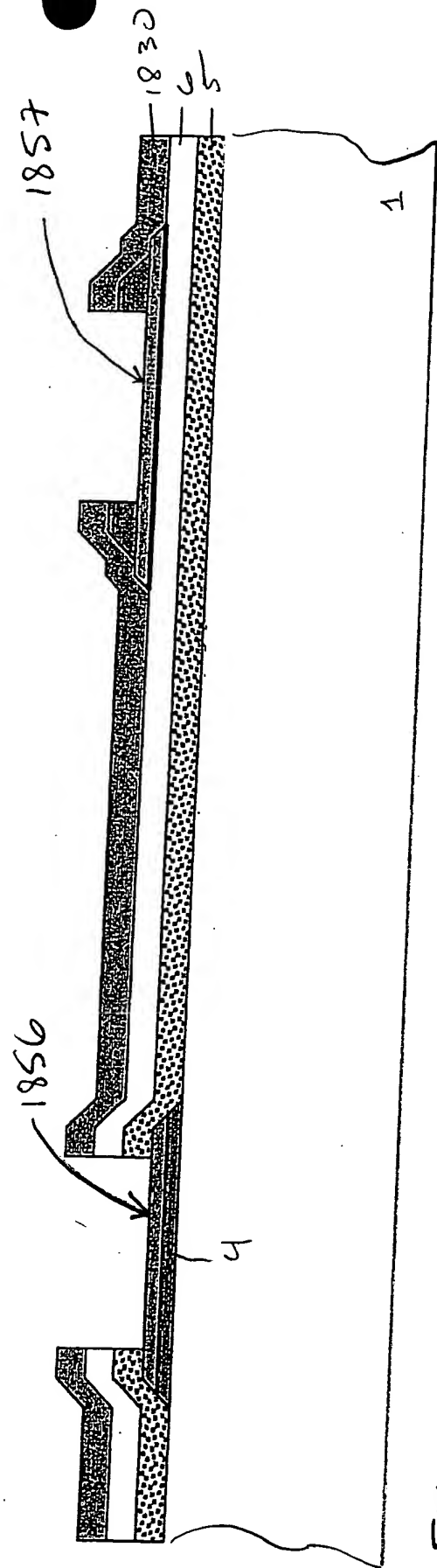


FIG 20L

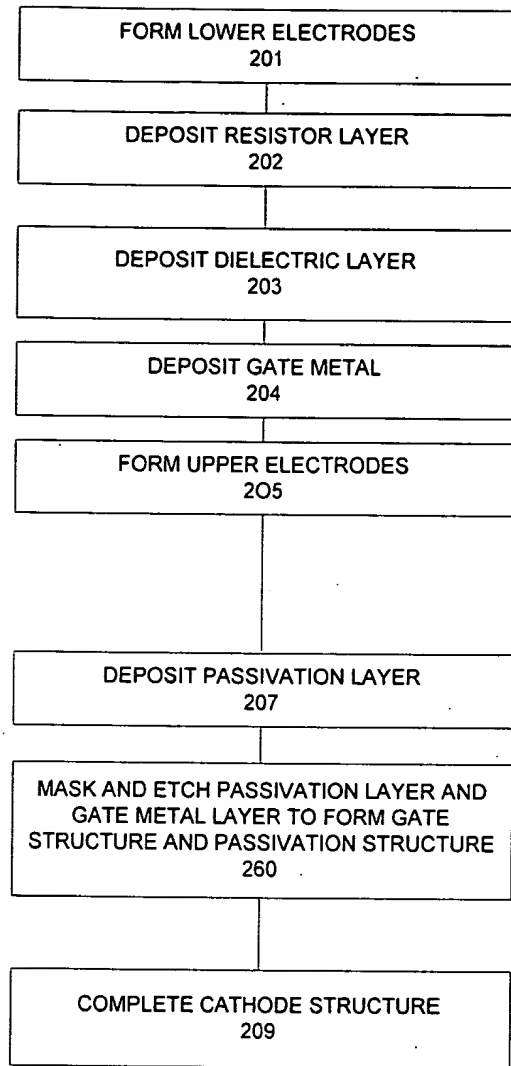


FIG. 21

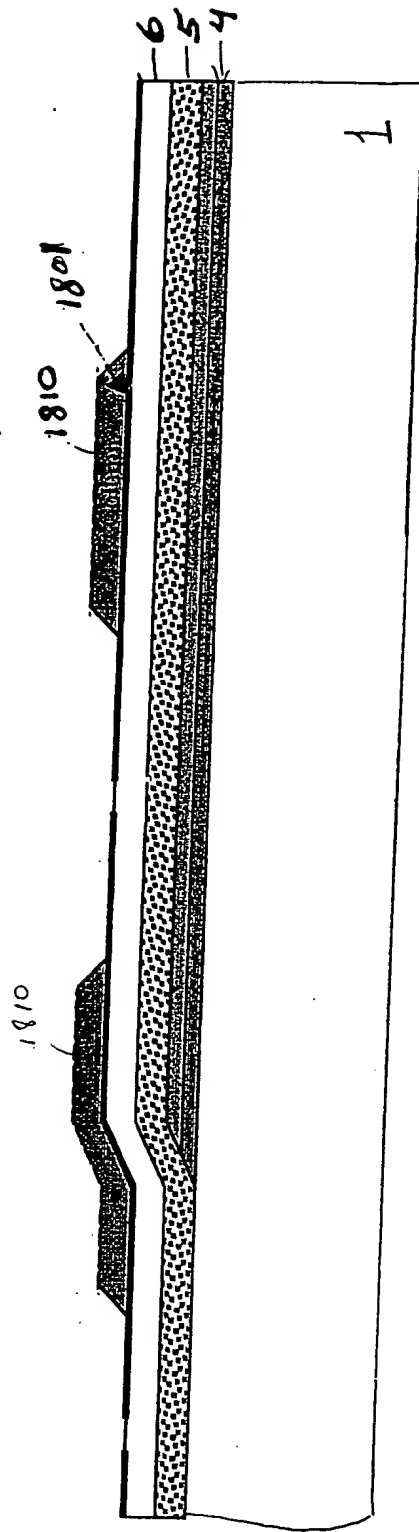


FIG. 22A

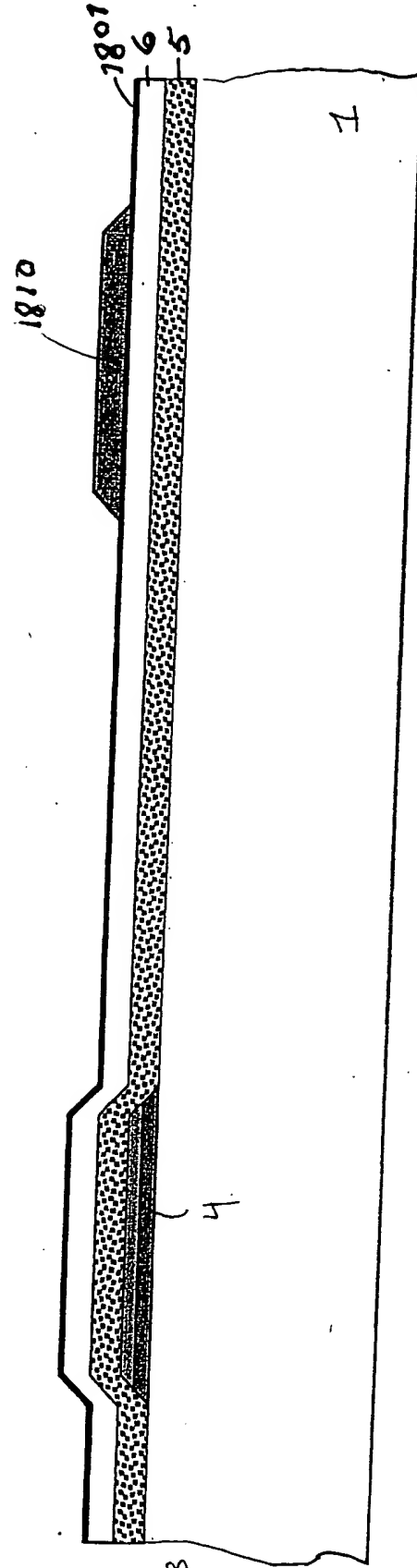


FIG. 22B

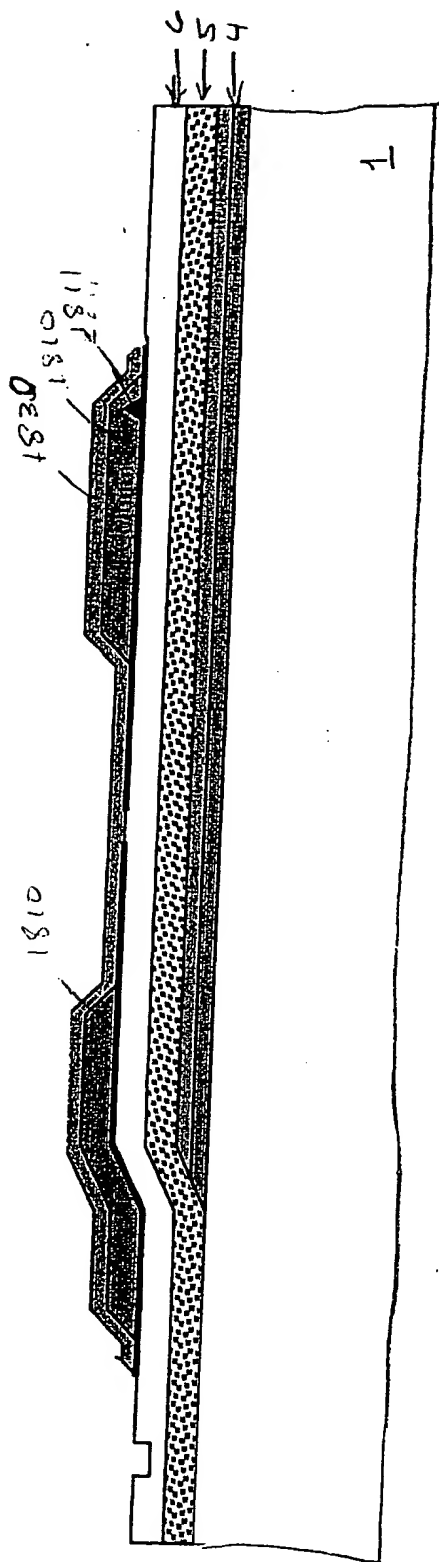


FIG. 22C

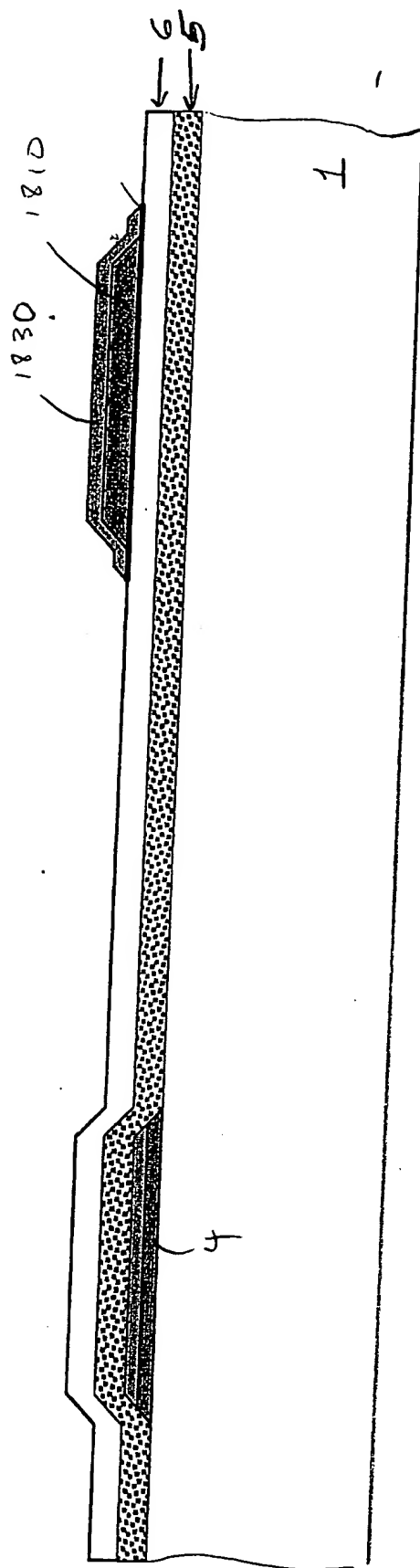


FIG. 22D

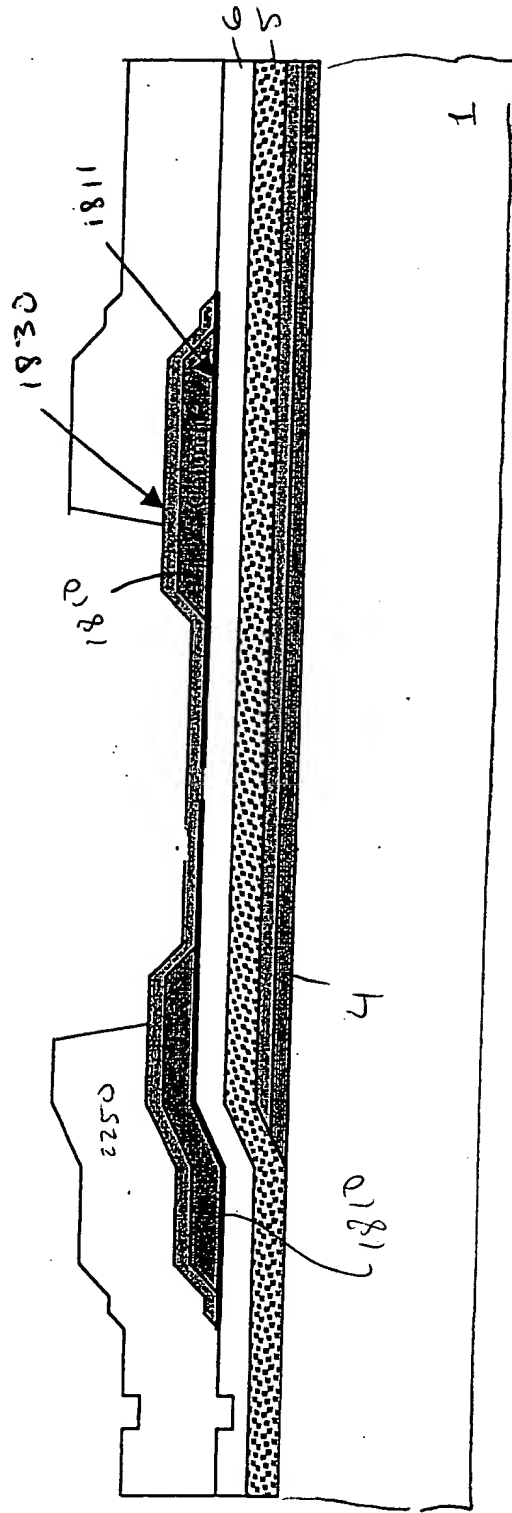


FIG 22E

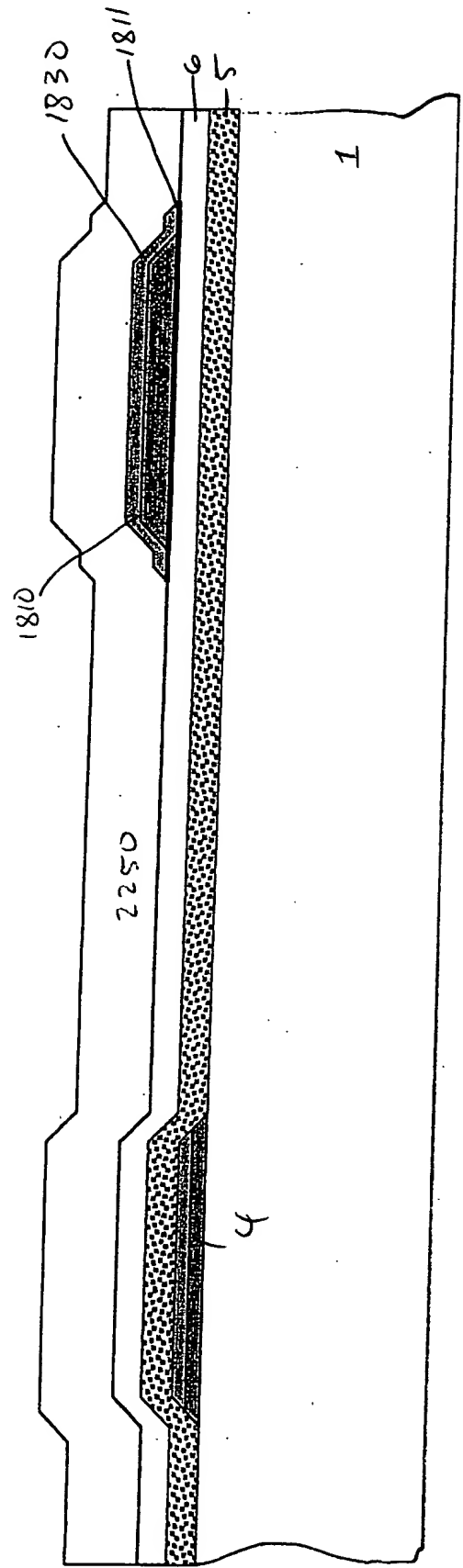


FIG 22F

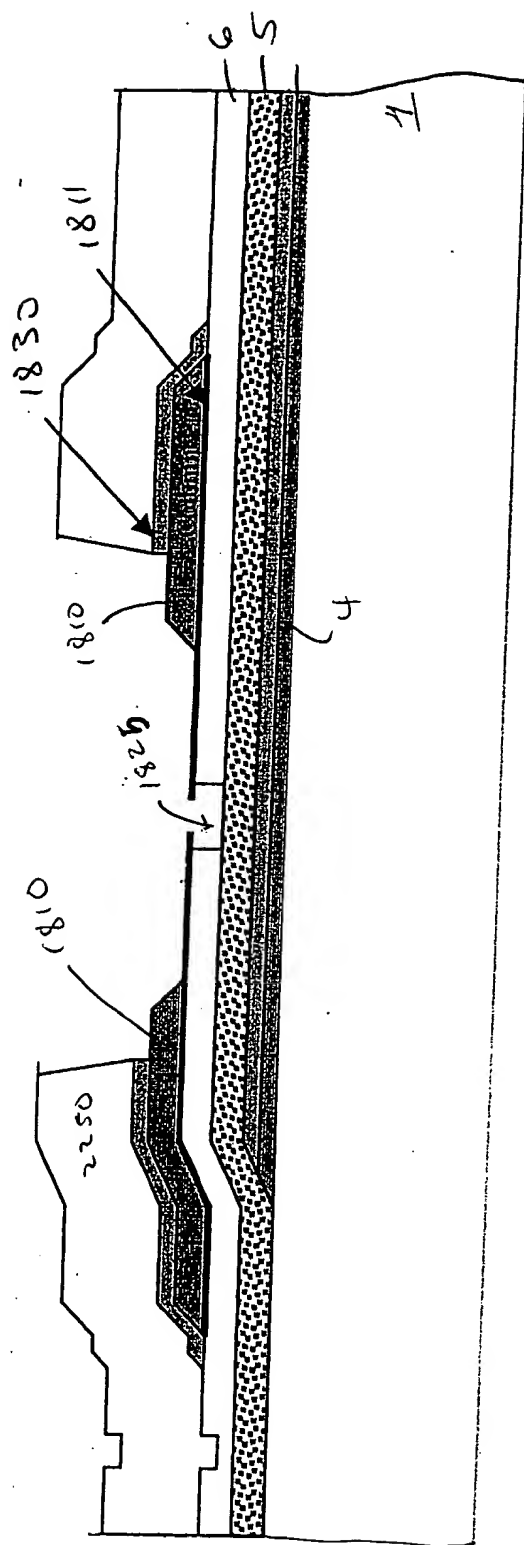


FIG 22C

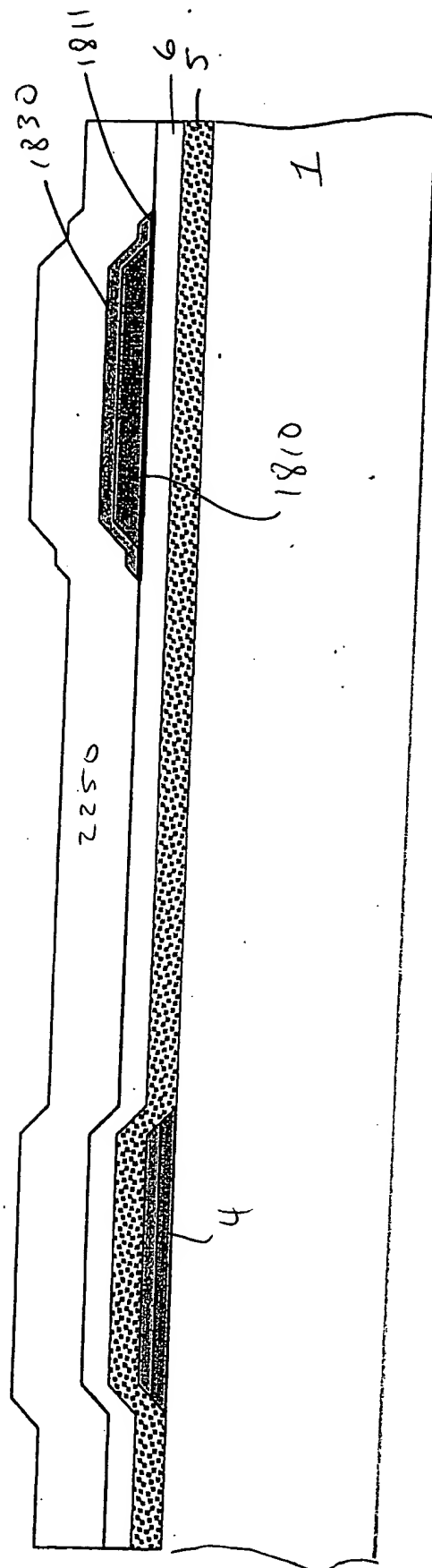


FIG 22H

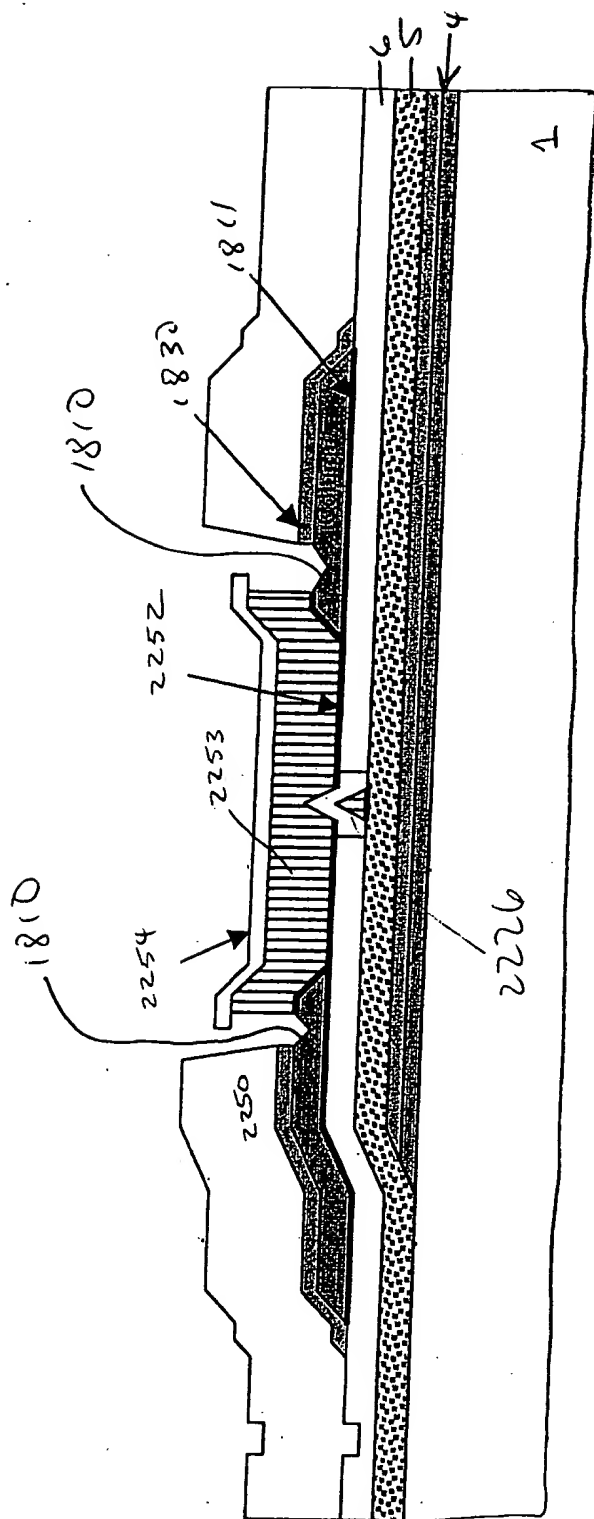
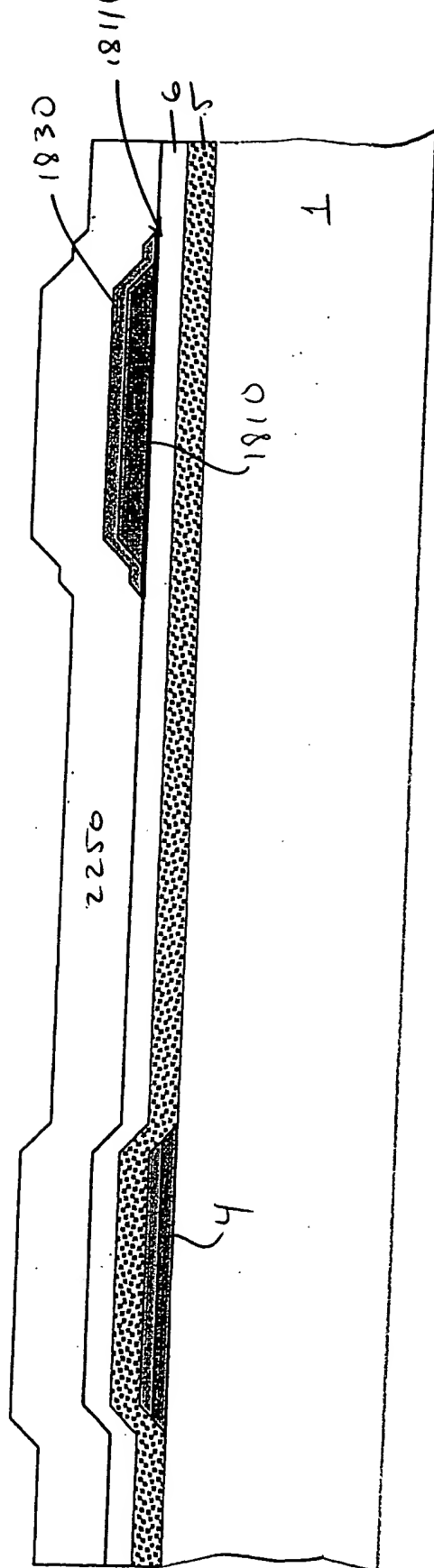
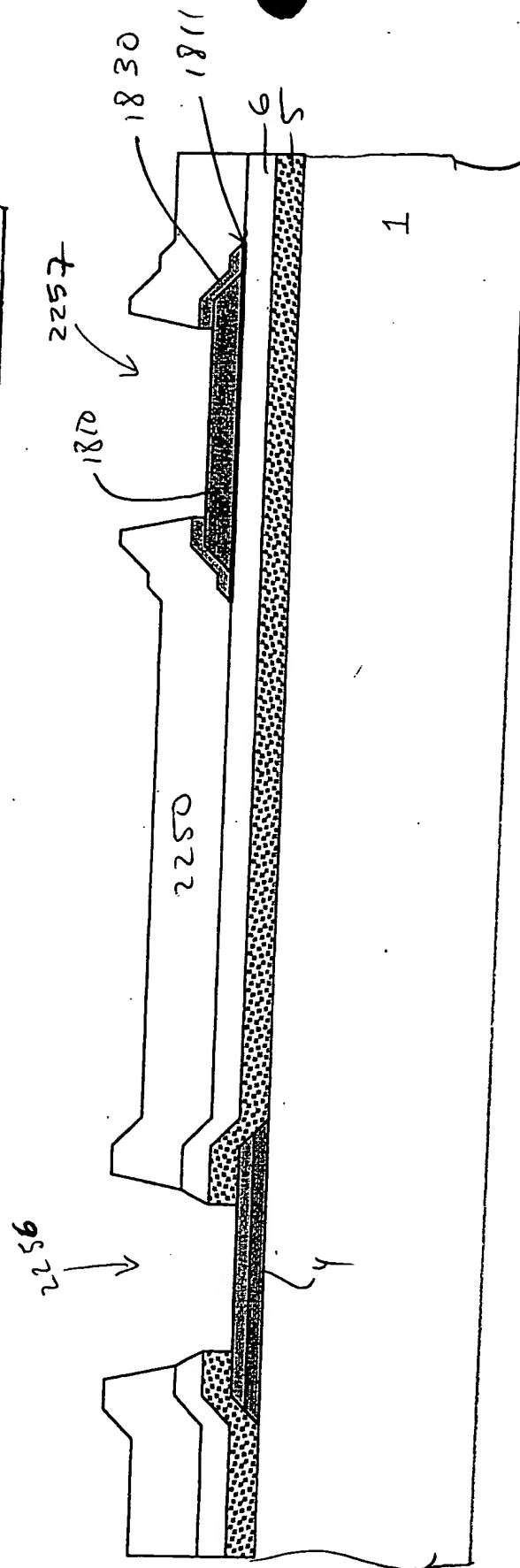
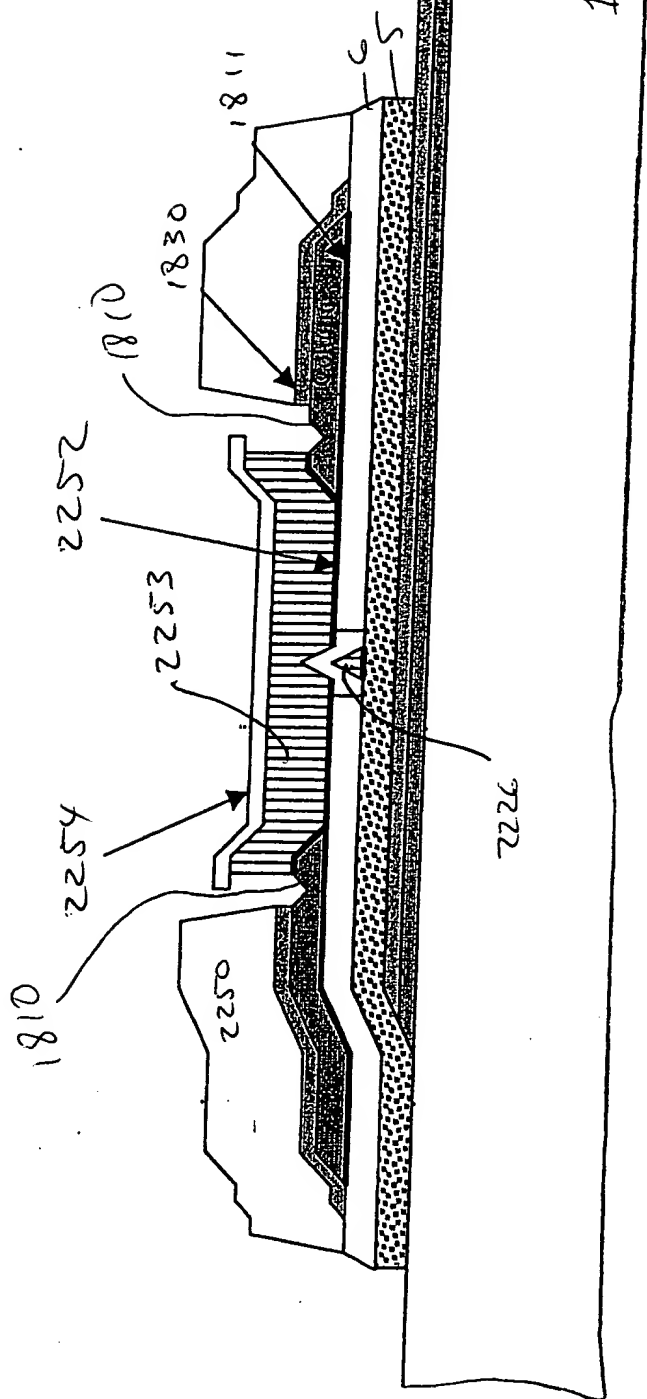
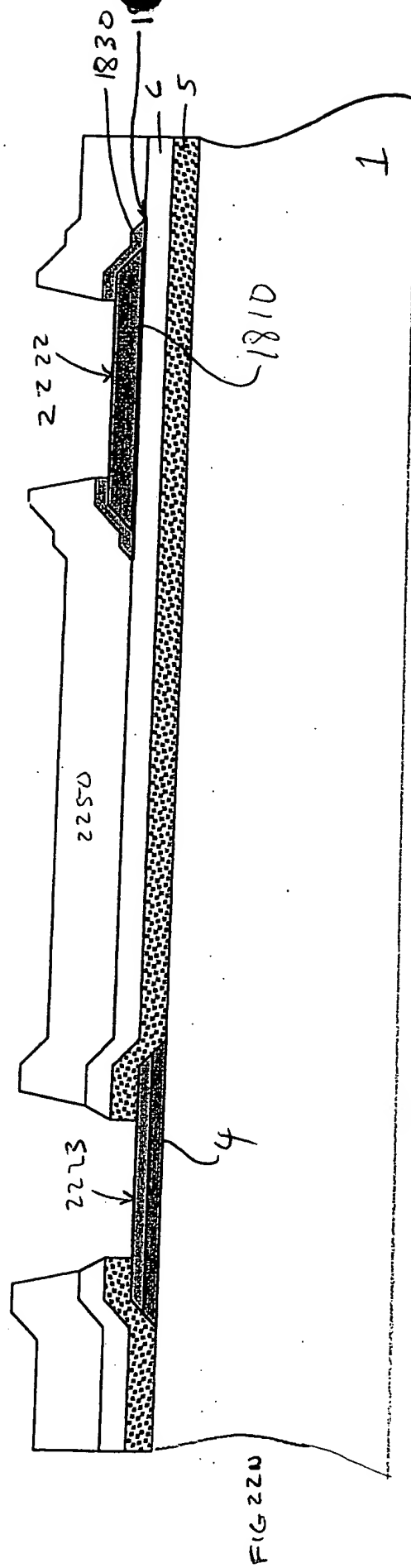
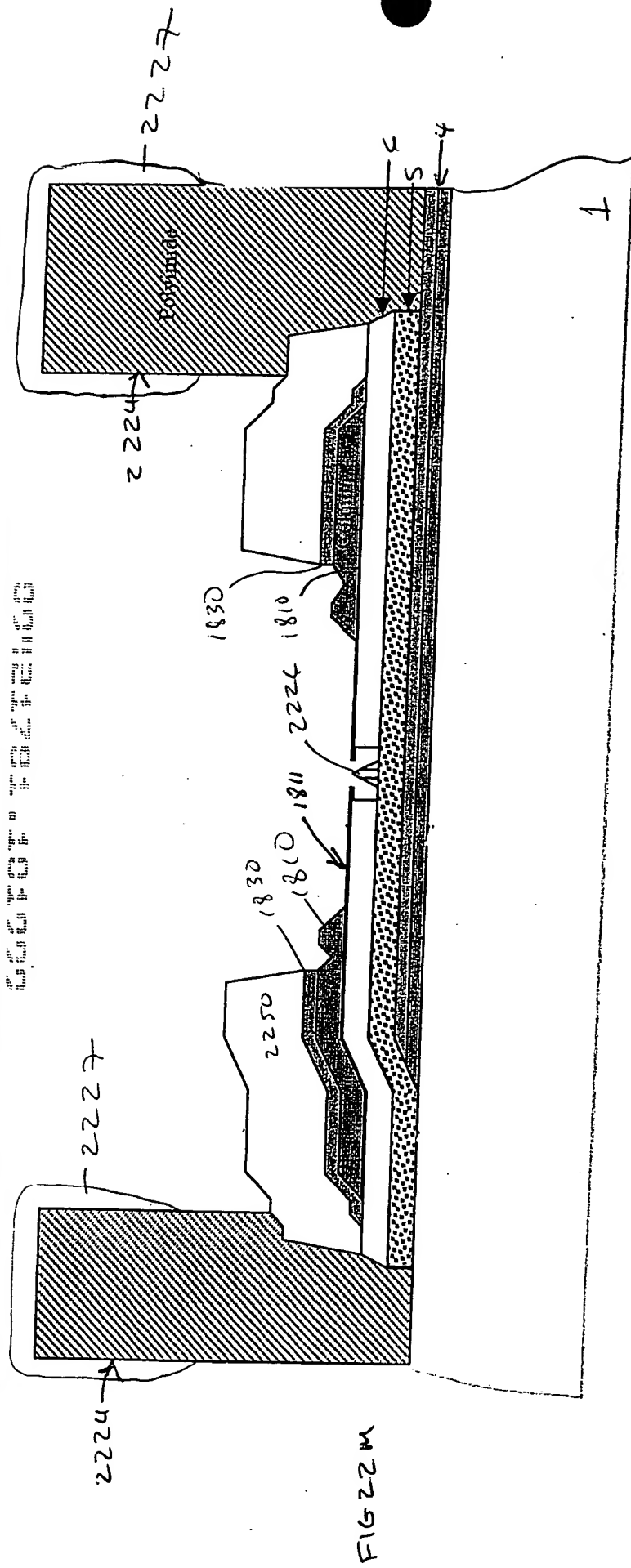


FIG. 22 I



522.913





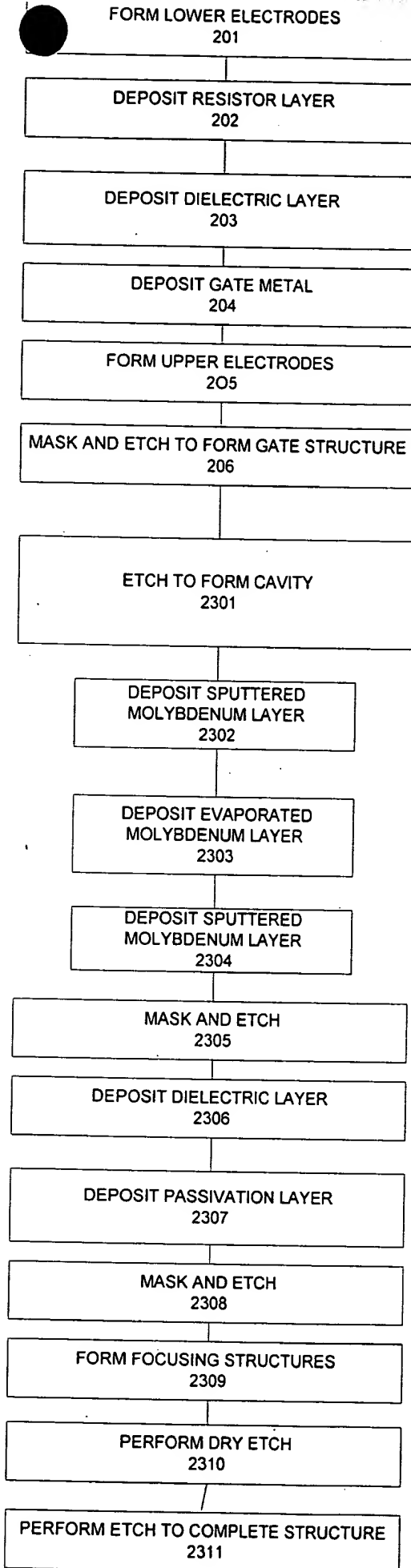


FIG. 23

U.S. Pat. No. 4,231,000

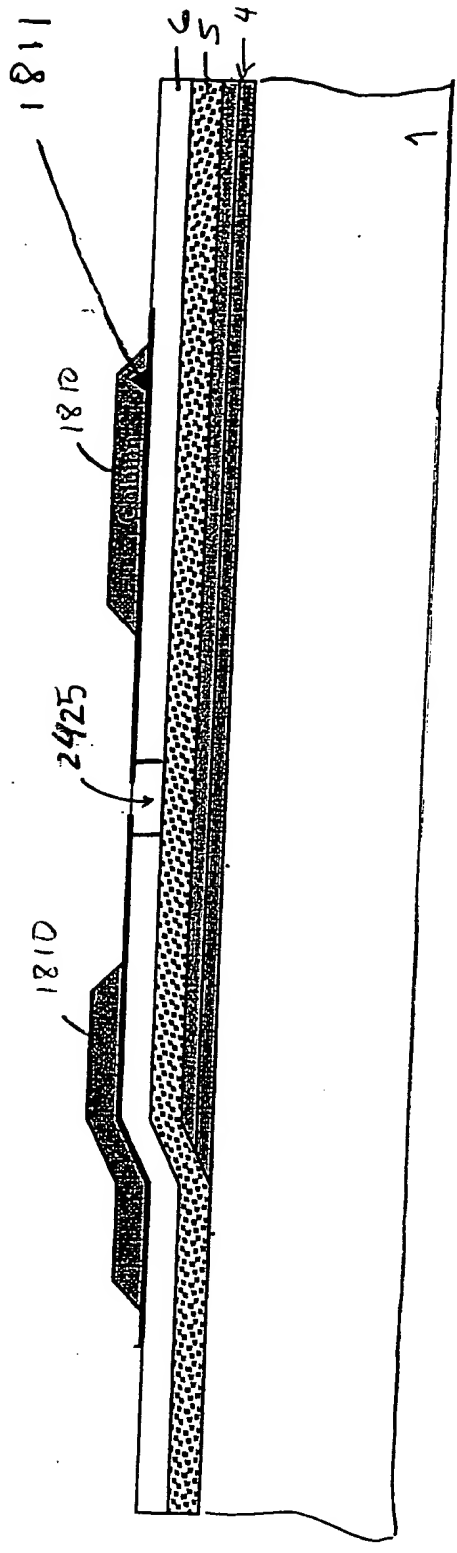


FIG 24A

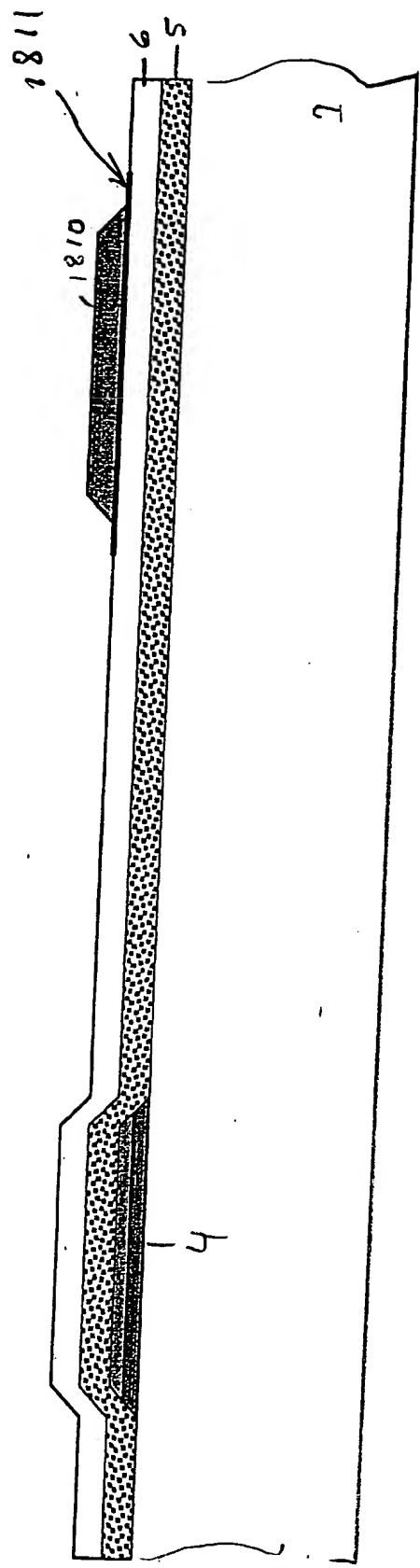


FIG. 24B

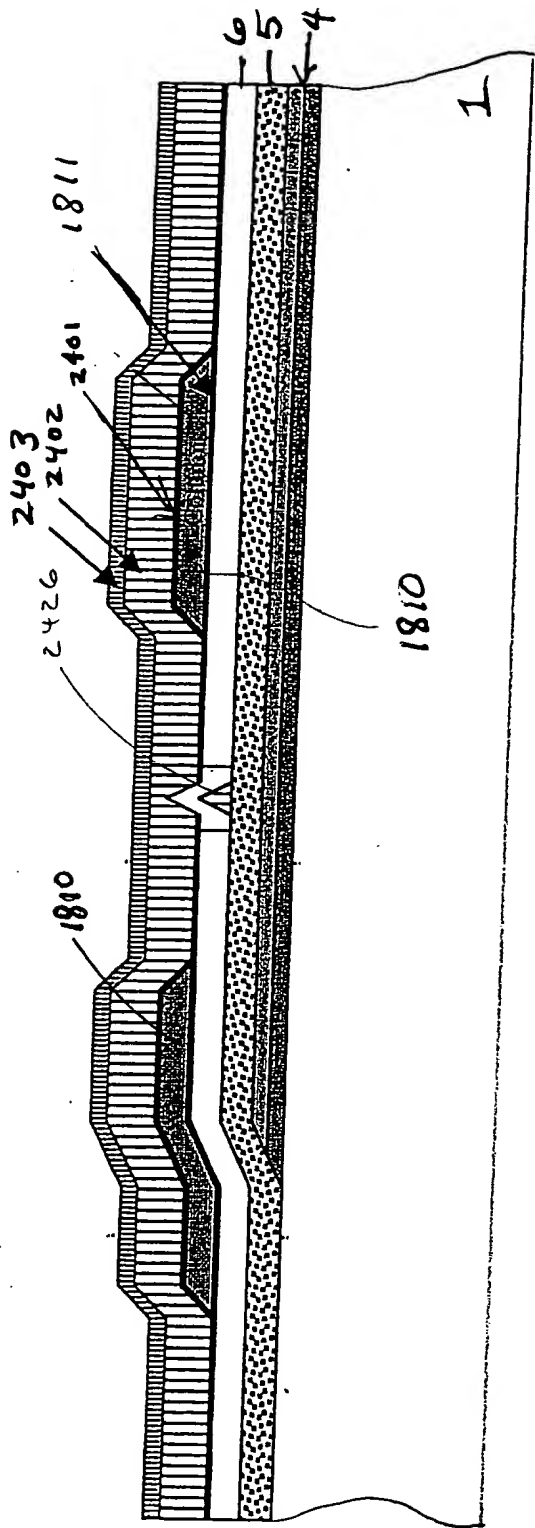


FIG. 24C

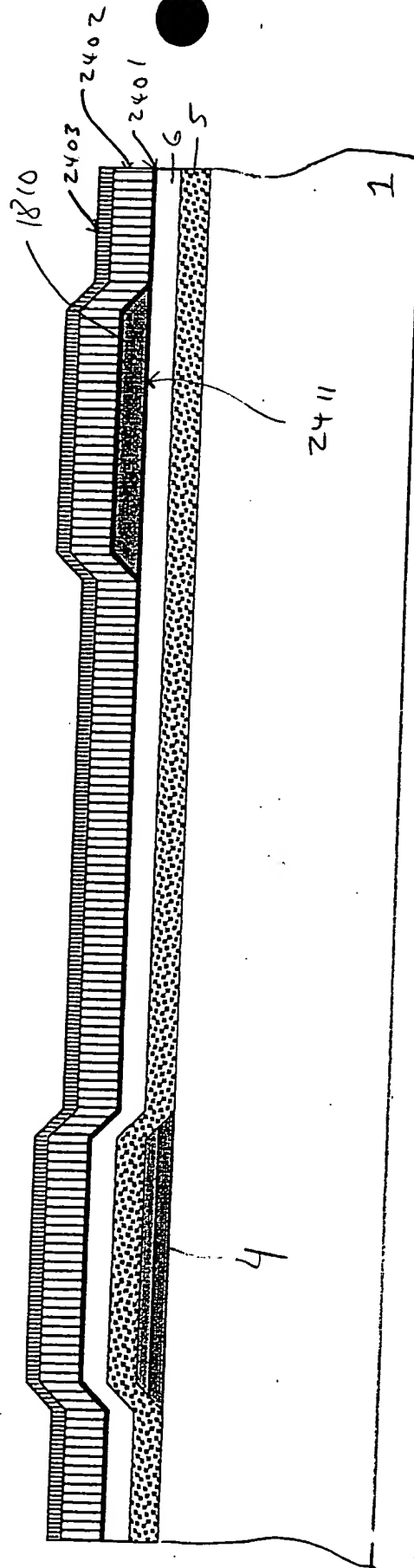
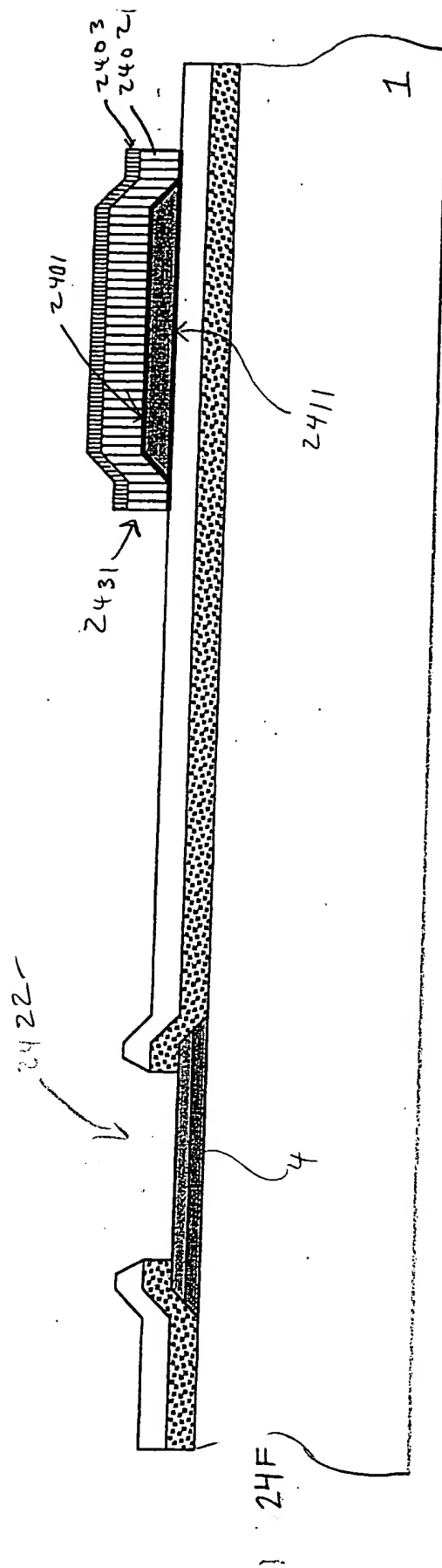
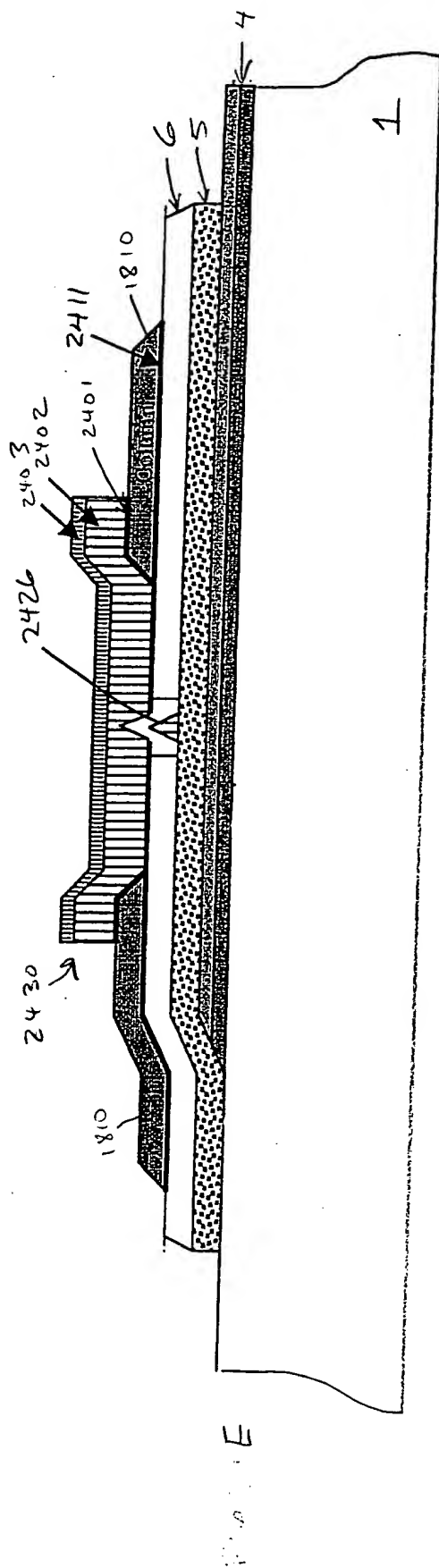
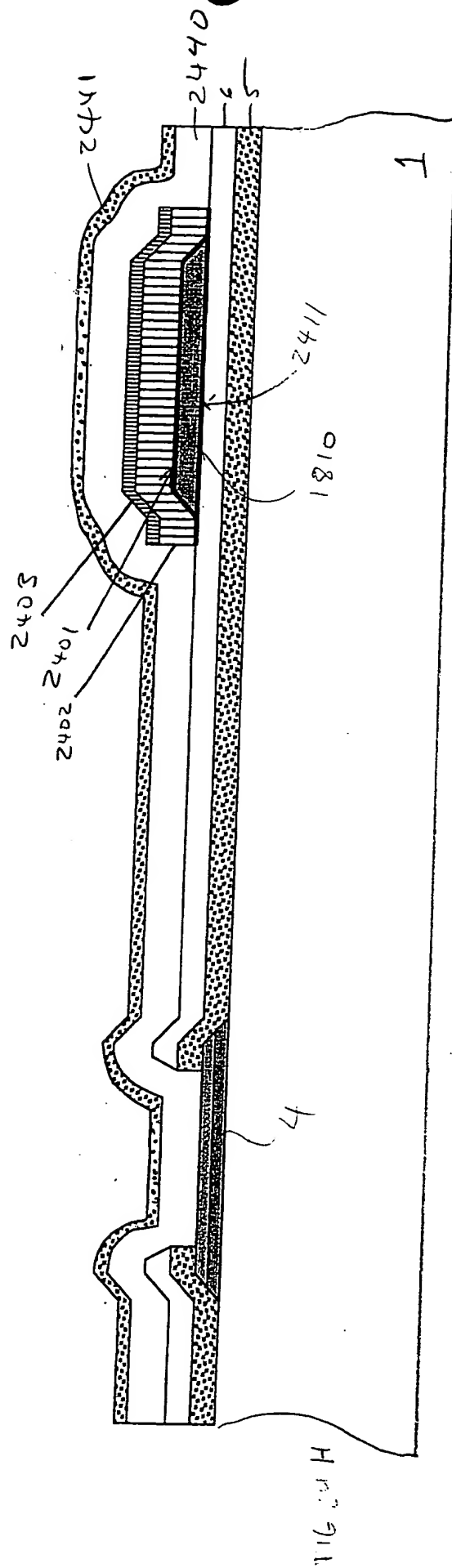
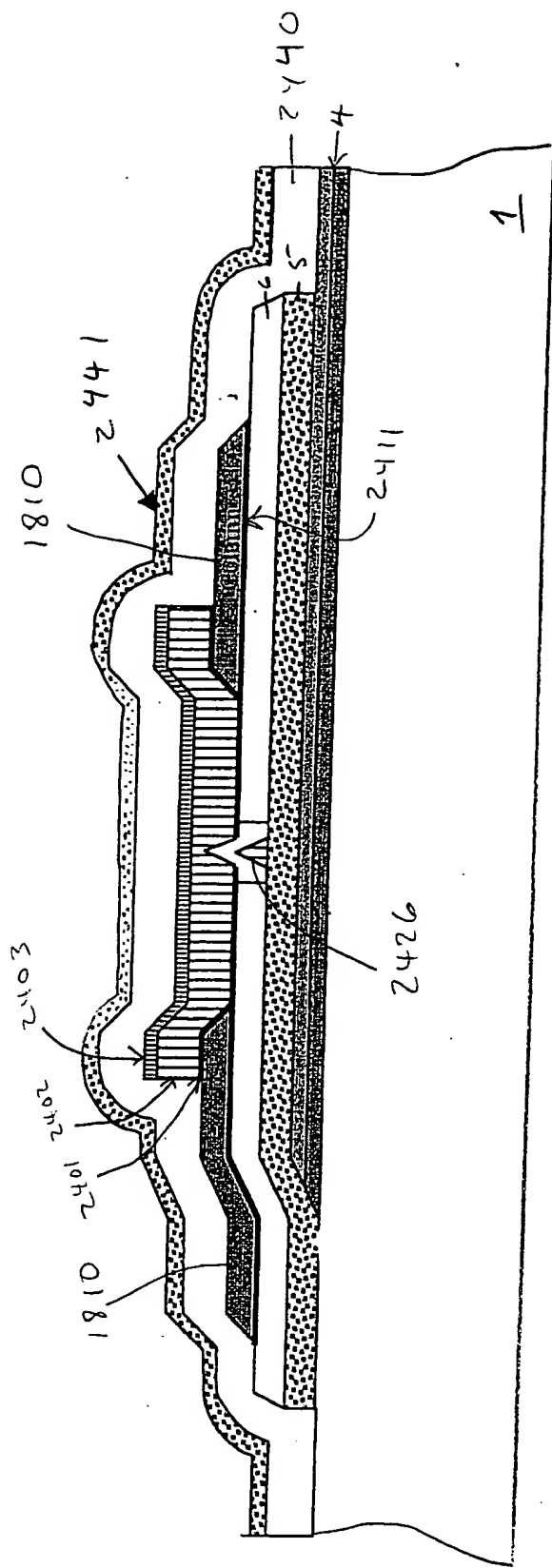
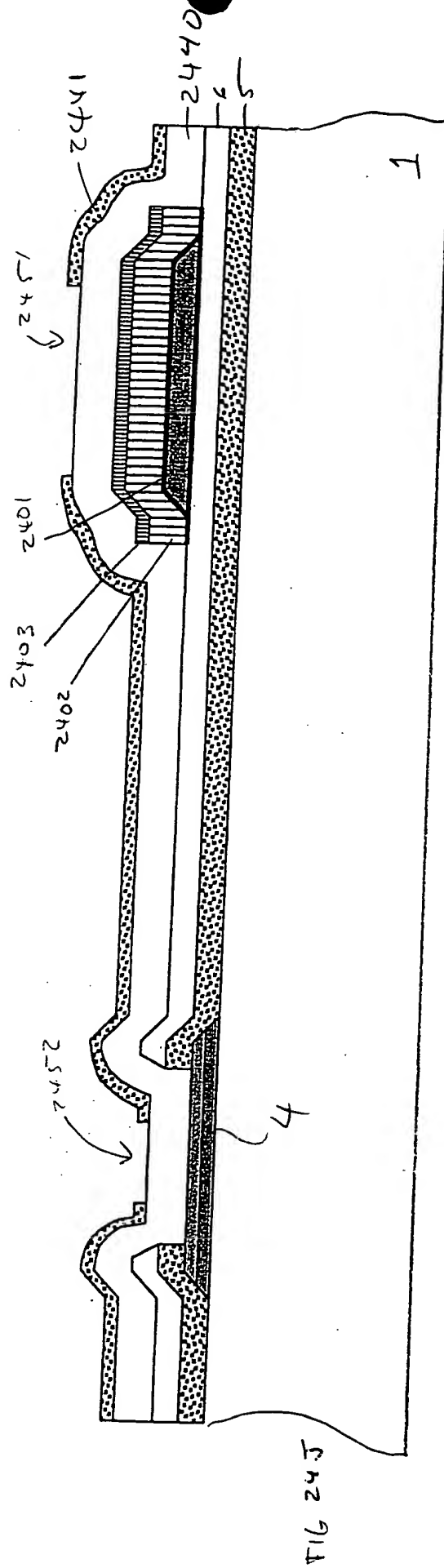
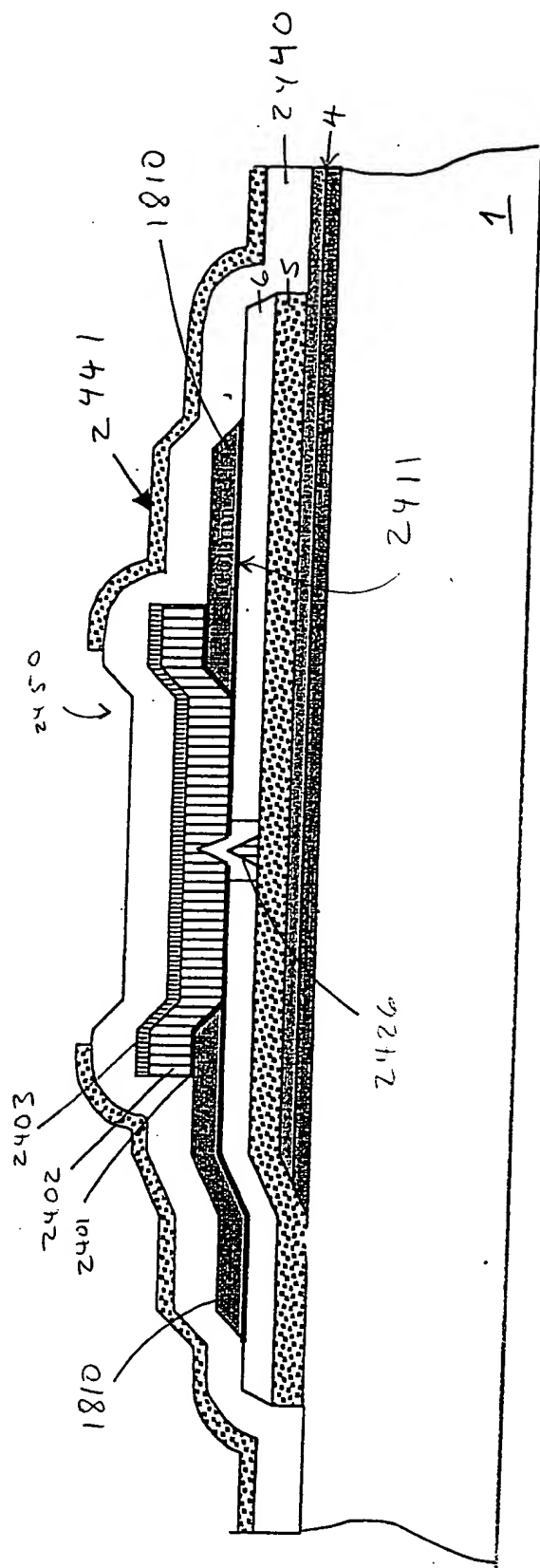


FIG. 24D







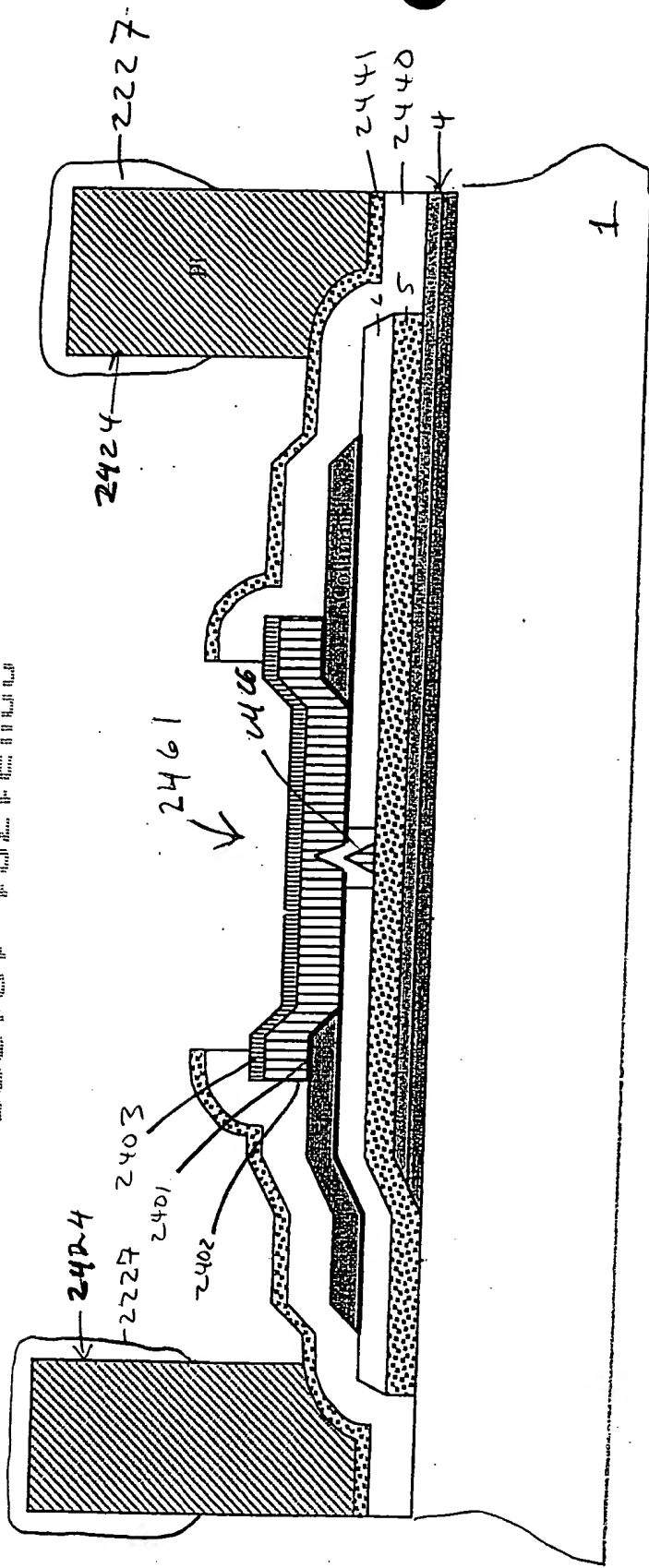


FIG 24K

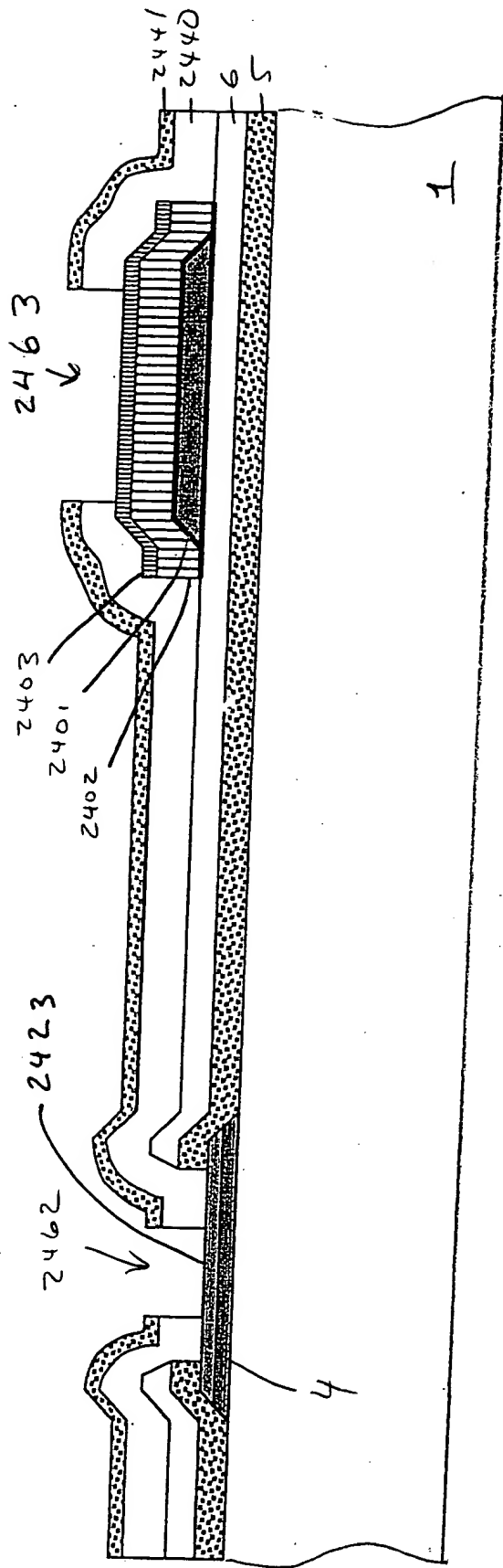


FIG 24L

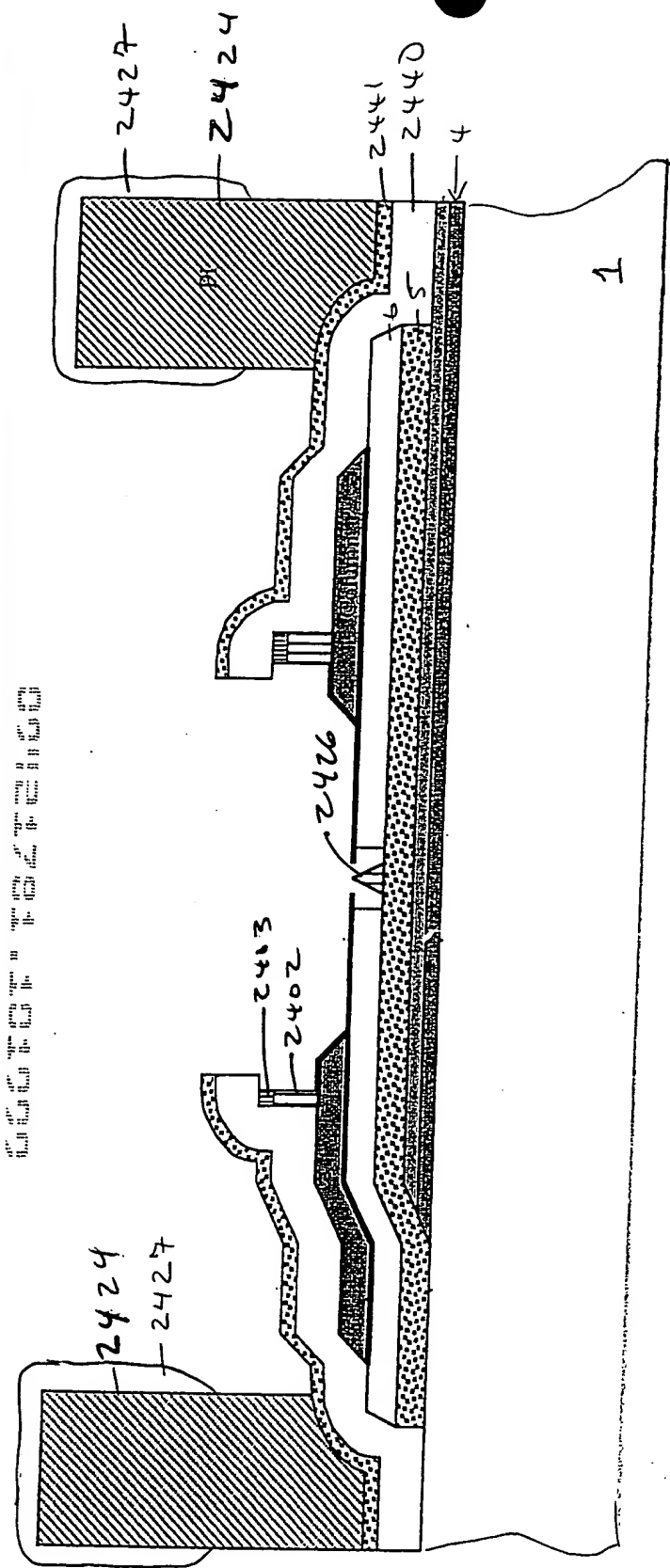


FIG. 24M

2422

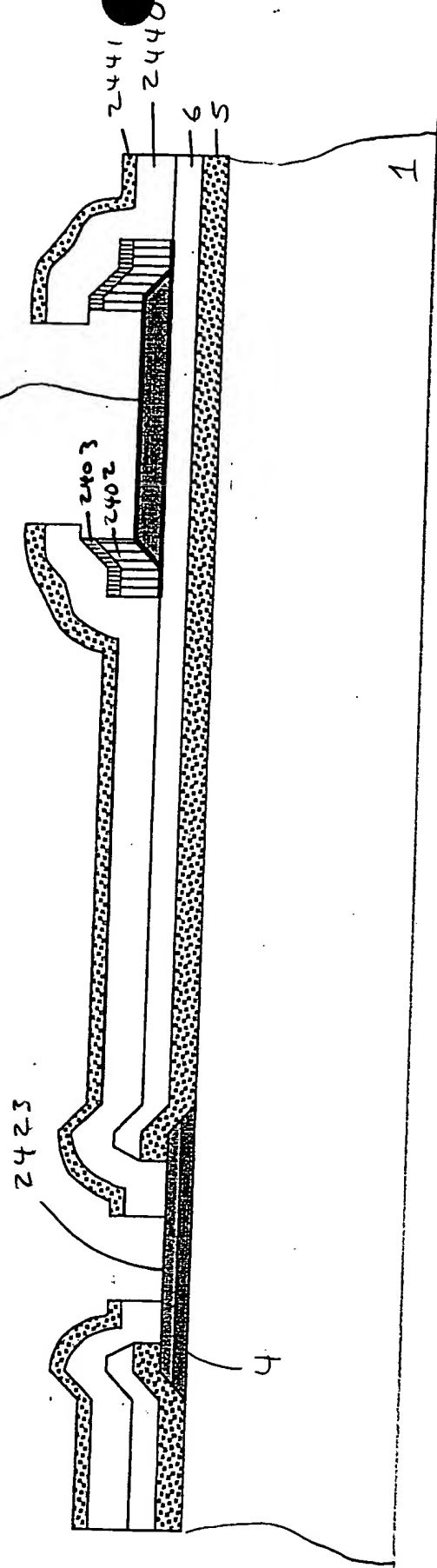


FIG. 24N

FIG. 25

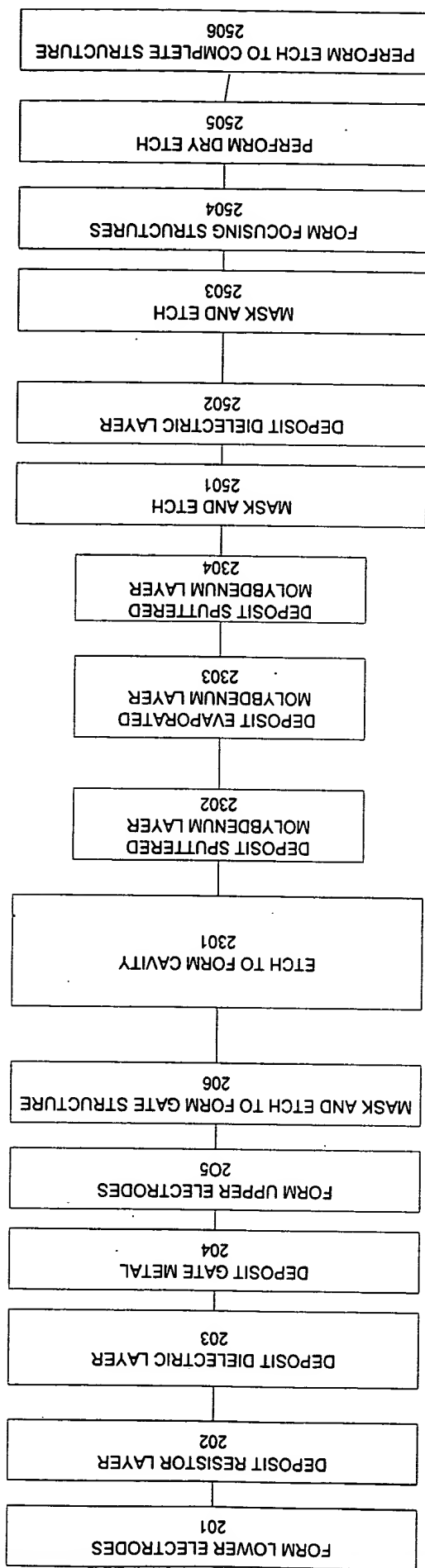


FIG. 25 is a flowchart of a semiconductor manufacturing process.

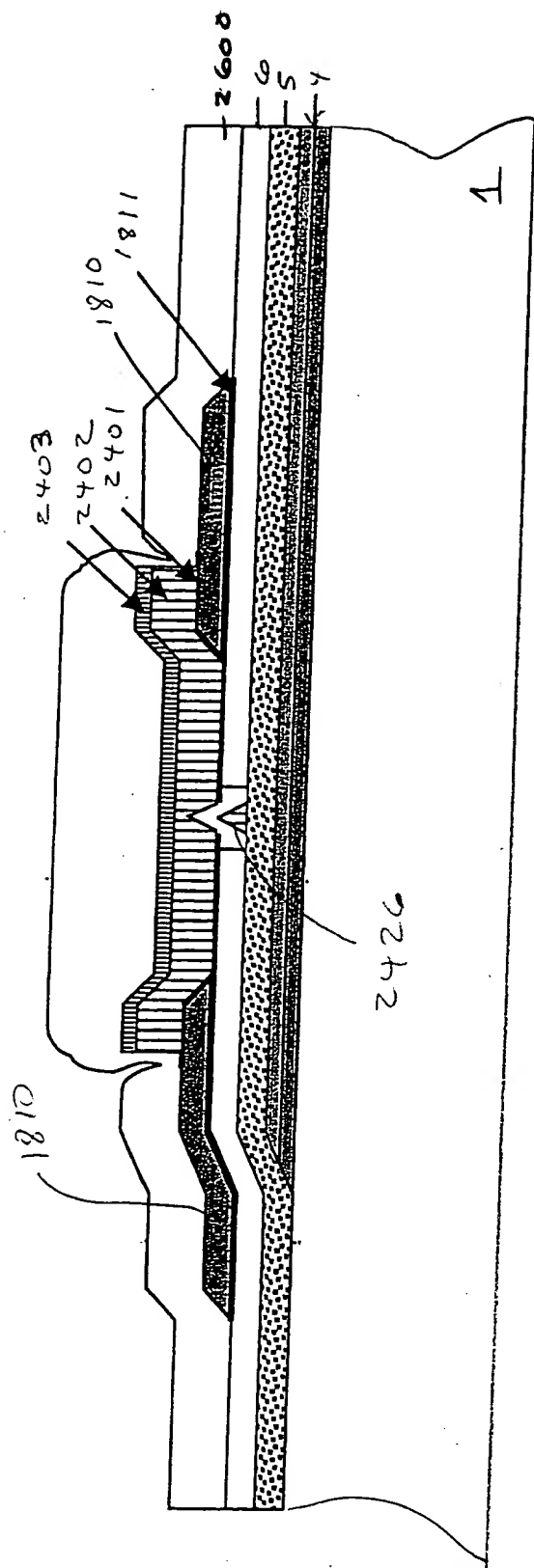
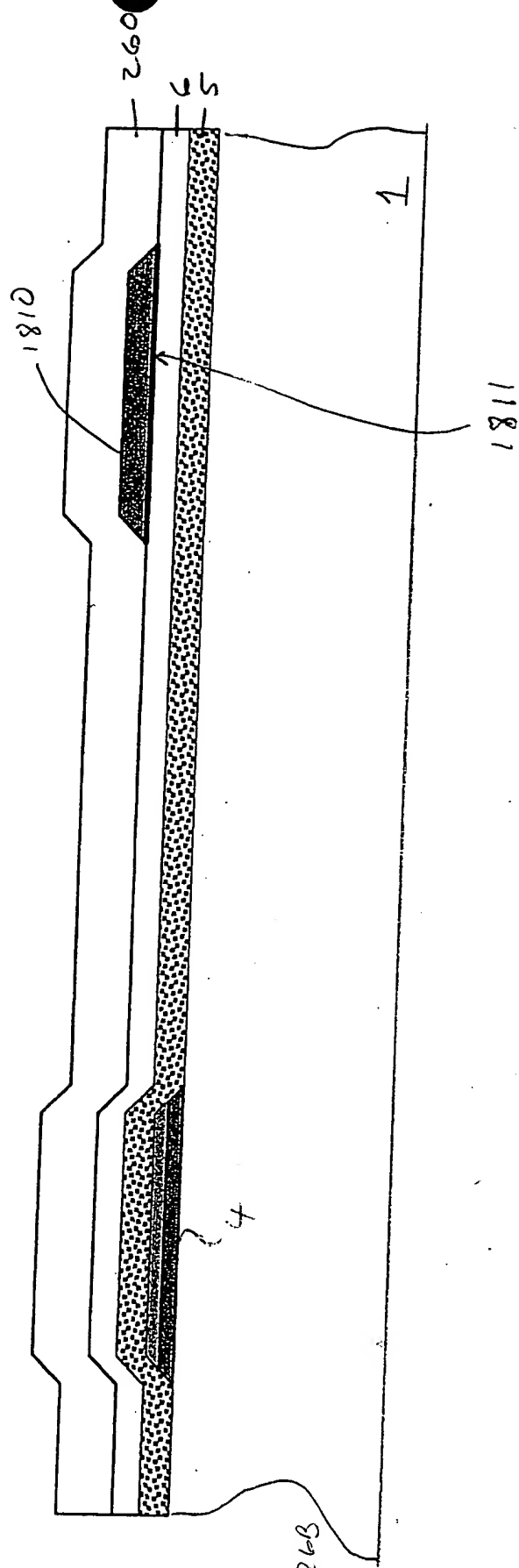


FIG. 26A



F.16.26B

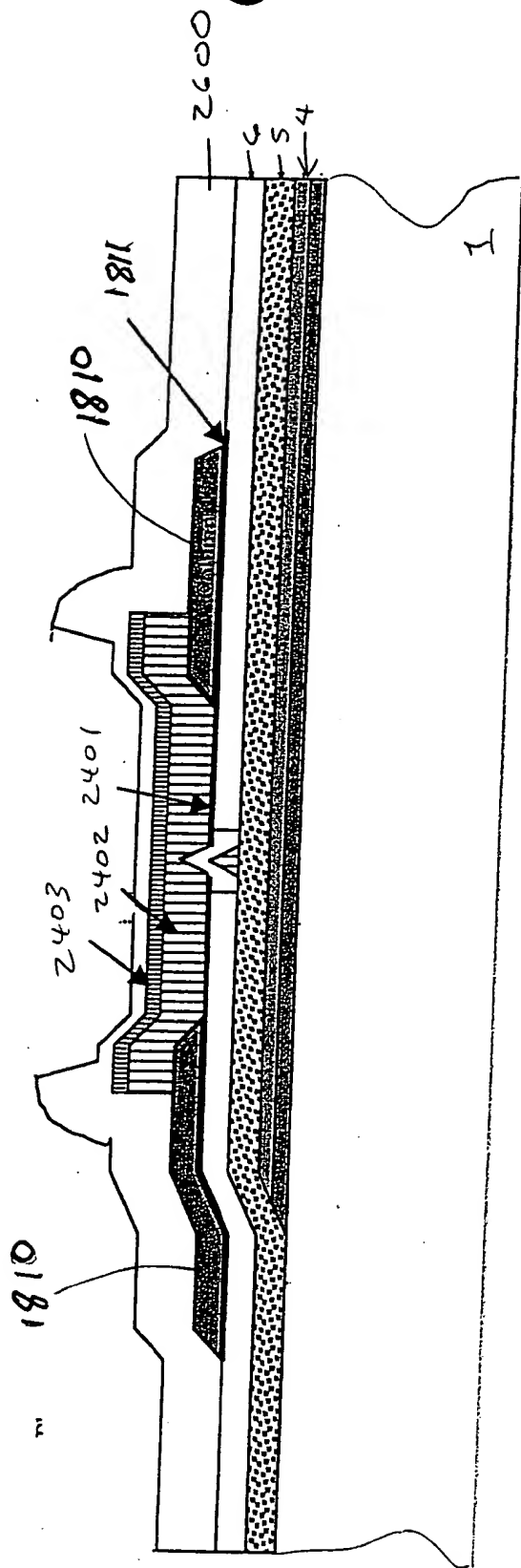


FIG 26C

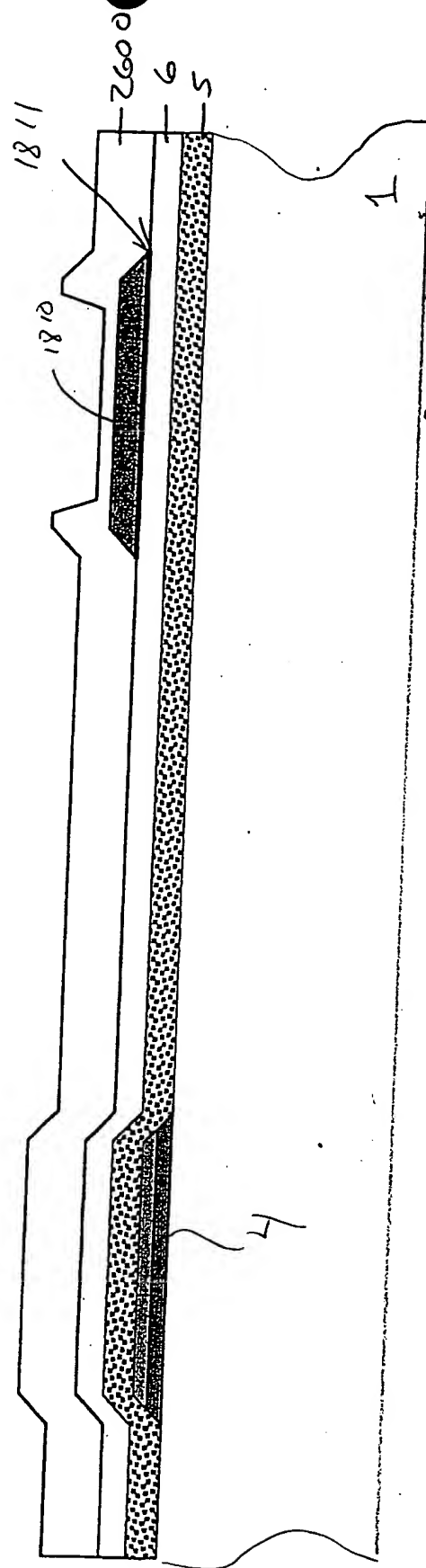
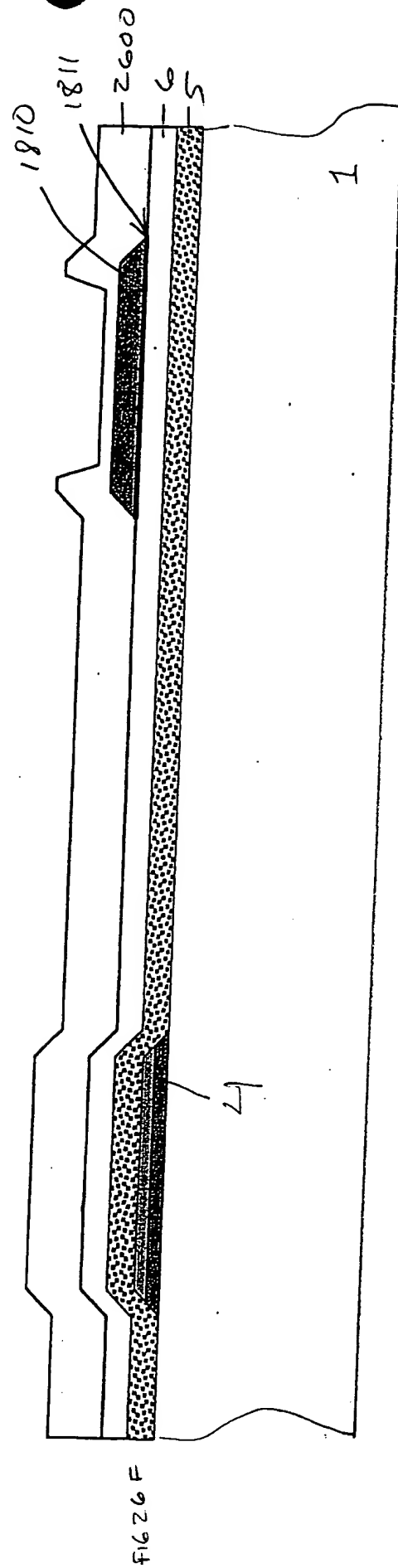
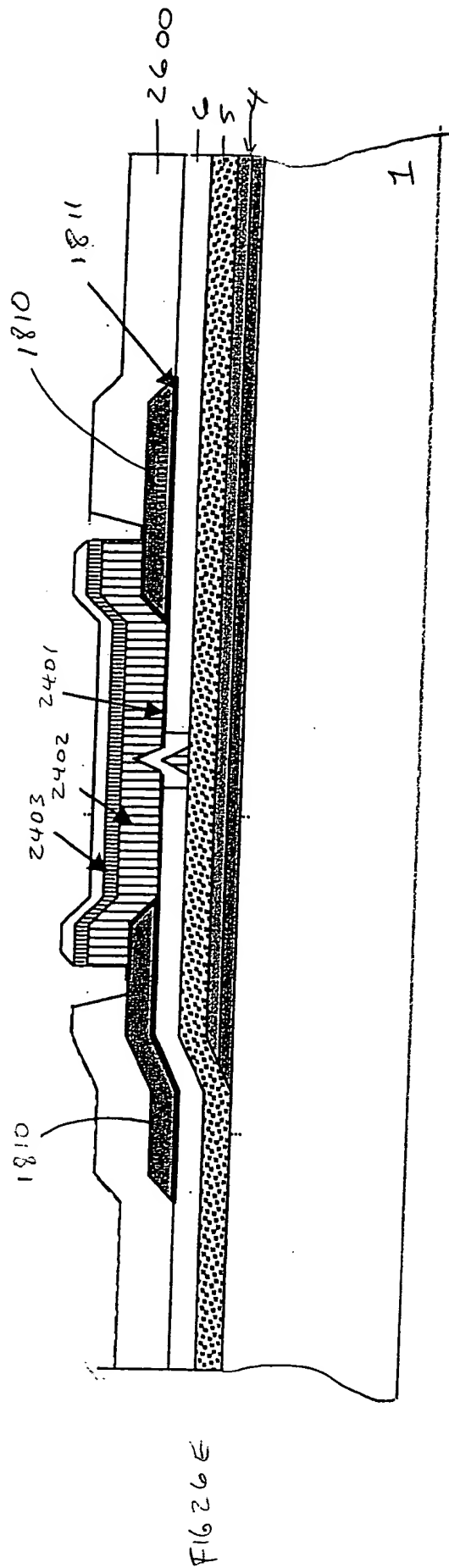


FIG 26D

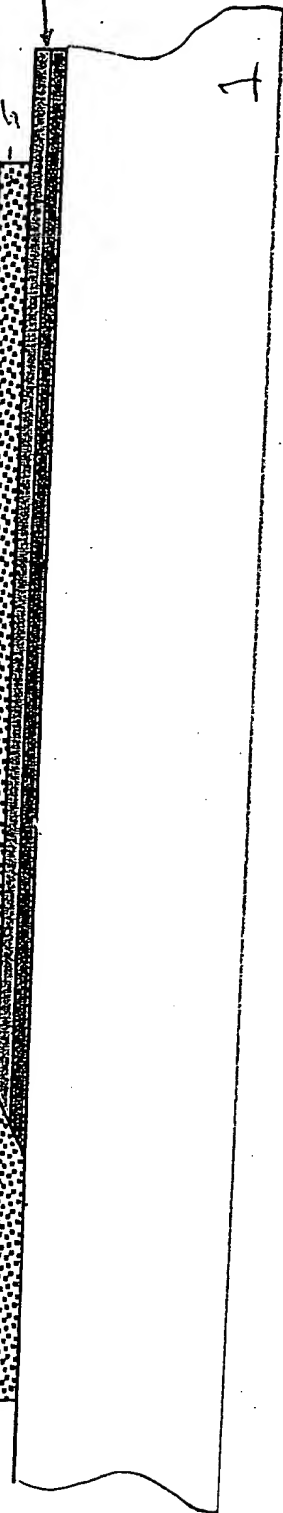


1

1810

2403/2402
2401
1811
2600
6
4

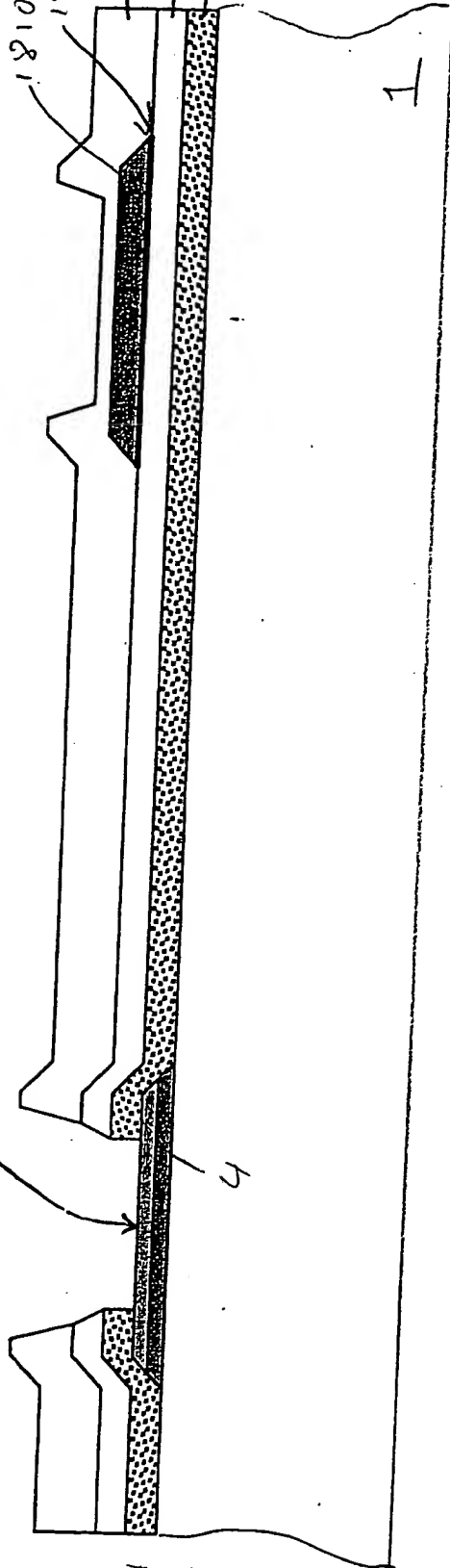
FIG. 26C

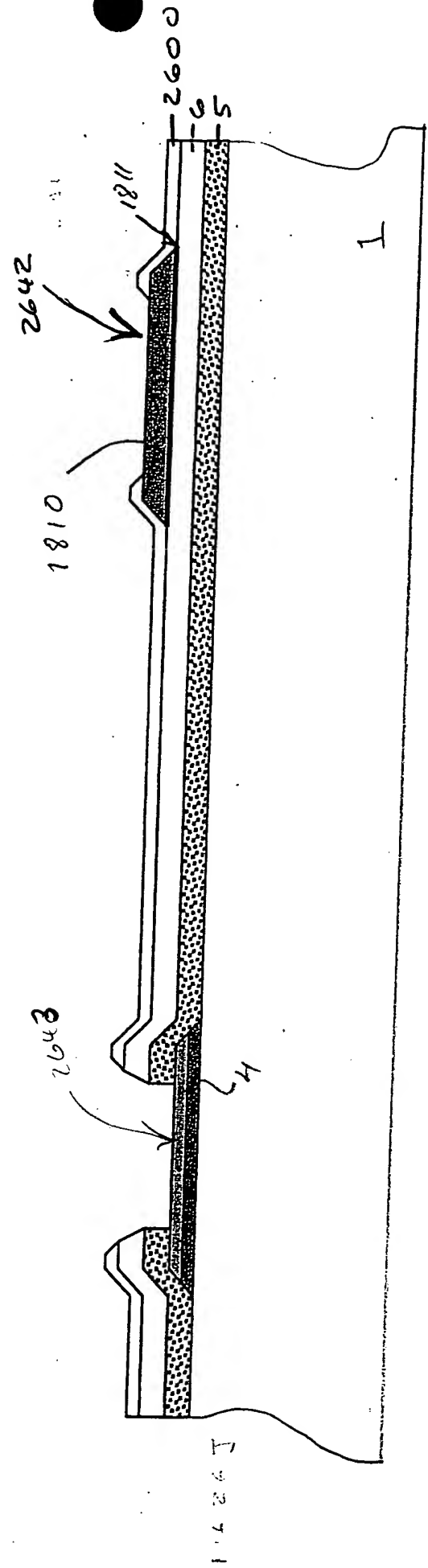
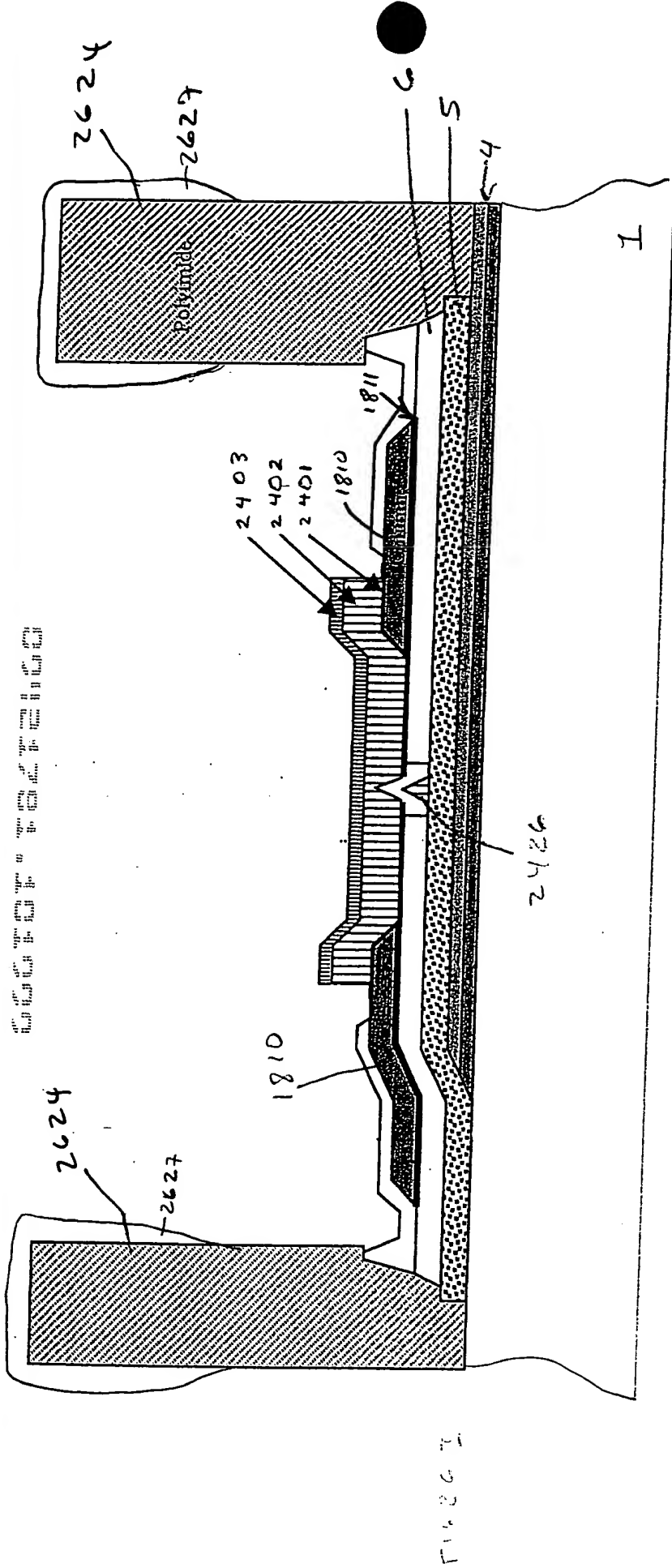


2643

1810
1811
2600
6
4

FIG. 26H





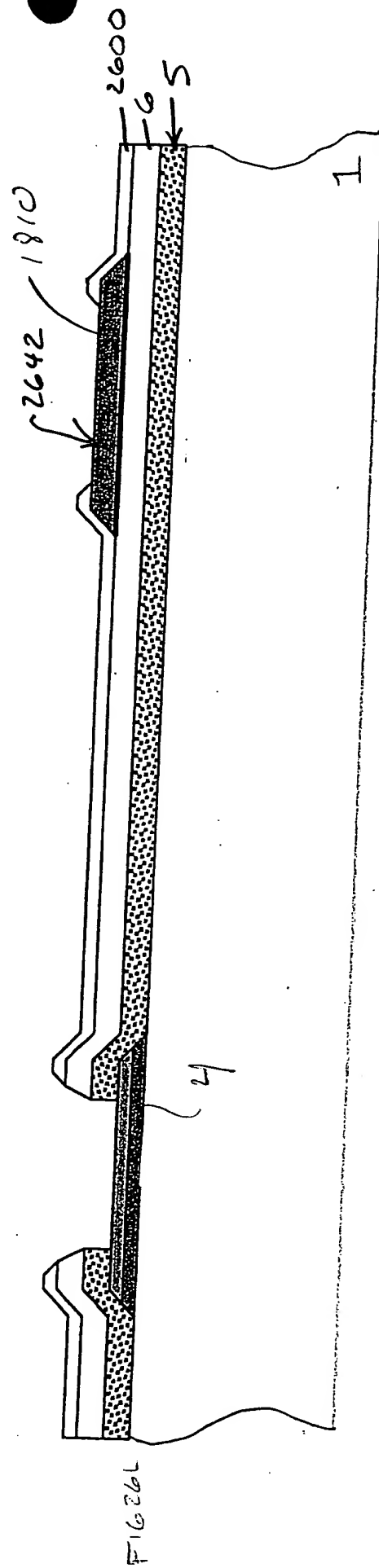
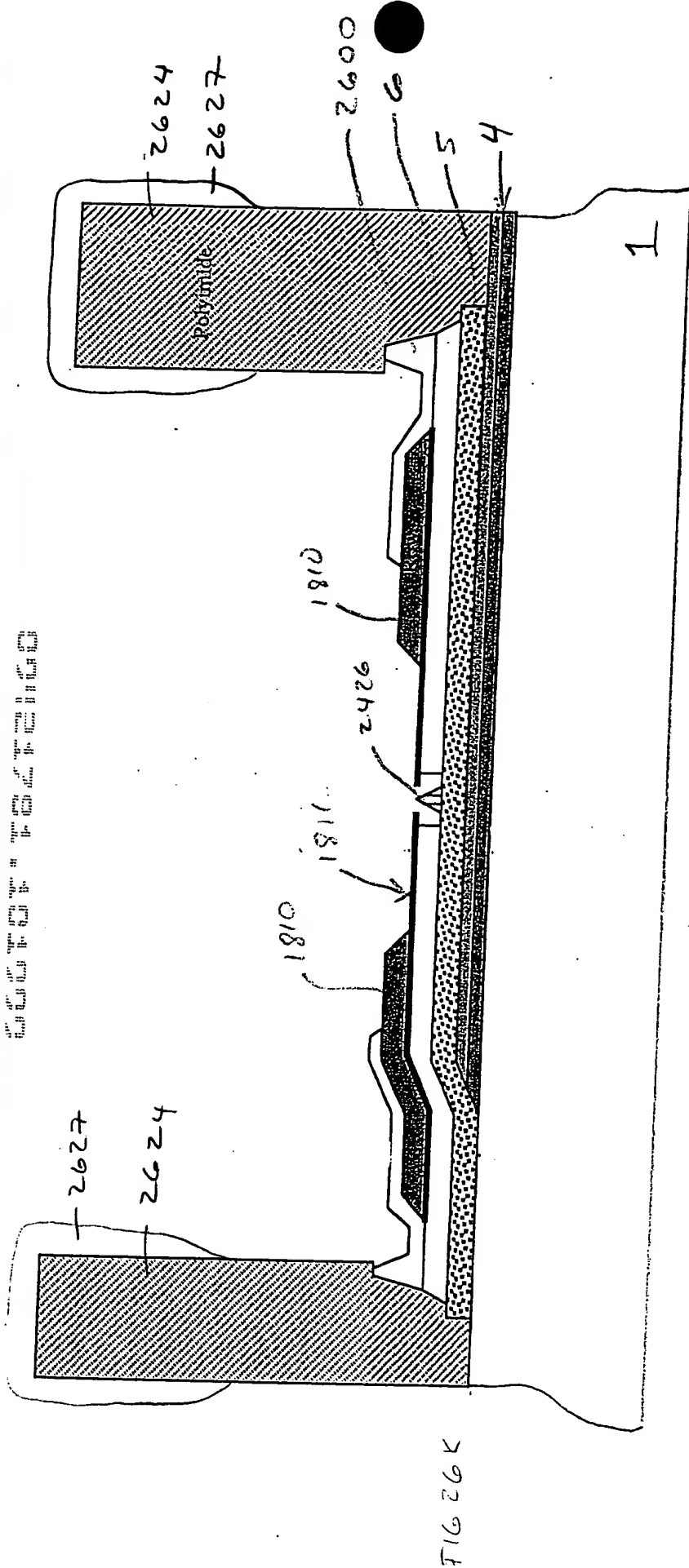


FIG. 27

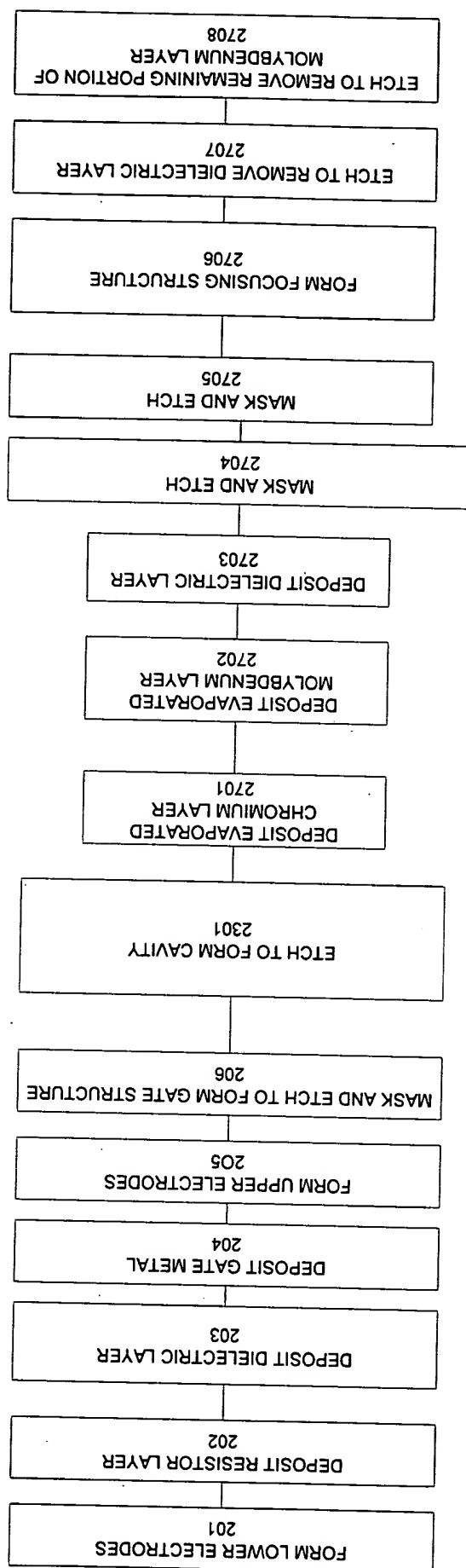


FIG. 27 is a flowchart of a method for forming a semiconductor device. The method includes forming lower electrodes (201), depositing a resistor layer (202), depositing a dielectric layer (203), depositing gate metal (204), forming upper electrodes (205), and masking and etching to form a gate structure (206). The method then includes etching to form a cavity (2301), depositing an evaporated chromium layer (2701), depositing an evaporated molybdenum layer (2702), depositing a dielectric layer (2703), masking and etching (2704), masking and etching (2705), forming a focusing structure (2706), etching to remove a dielectric layer (2707), and etching to remove a remaining portion of a molybdenum layer (2708).

2832

2832
181
2832
2426
2832
181

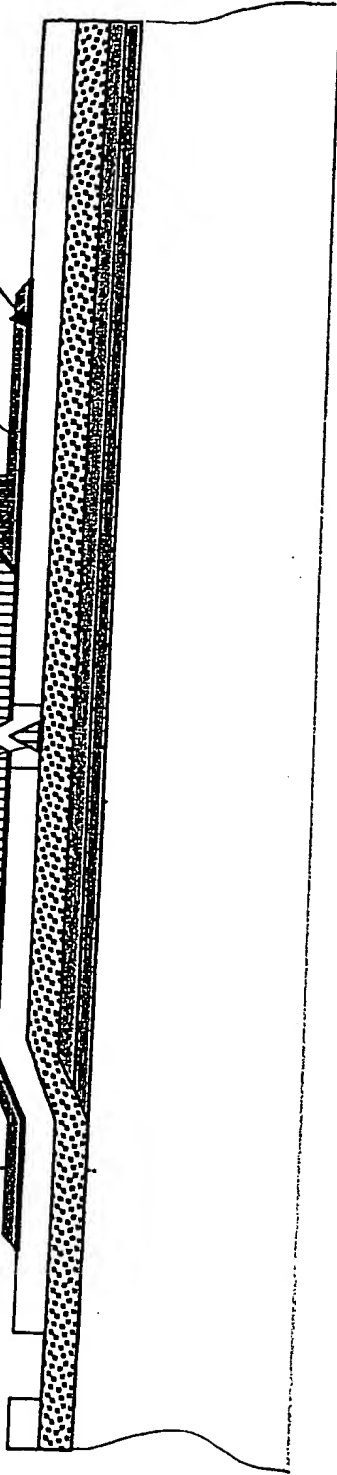


FIG 28C

2832
181
2832
181
2832
181

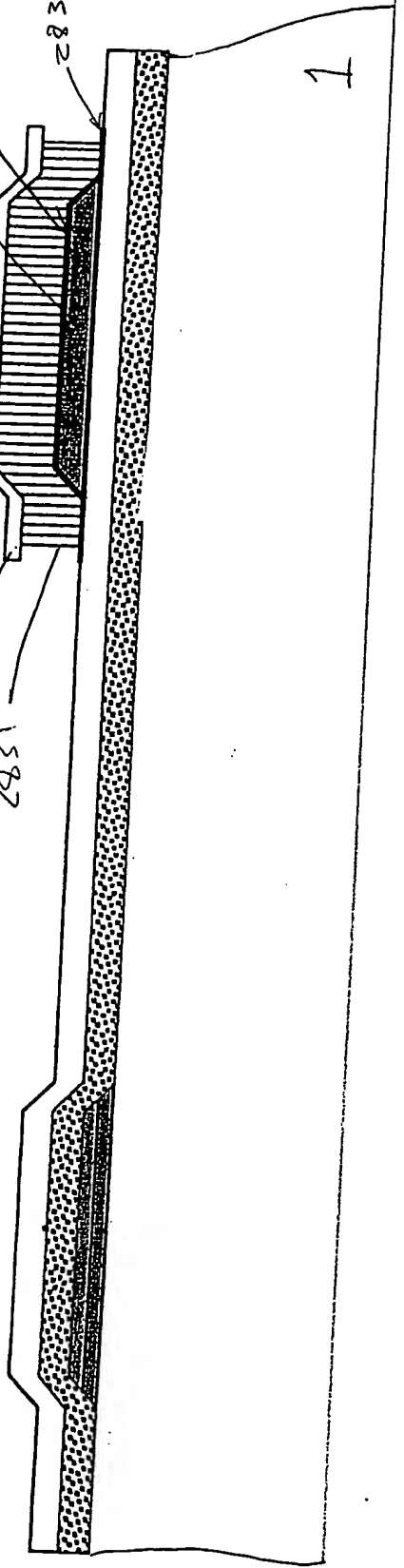
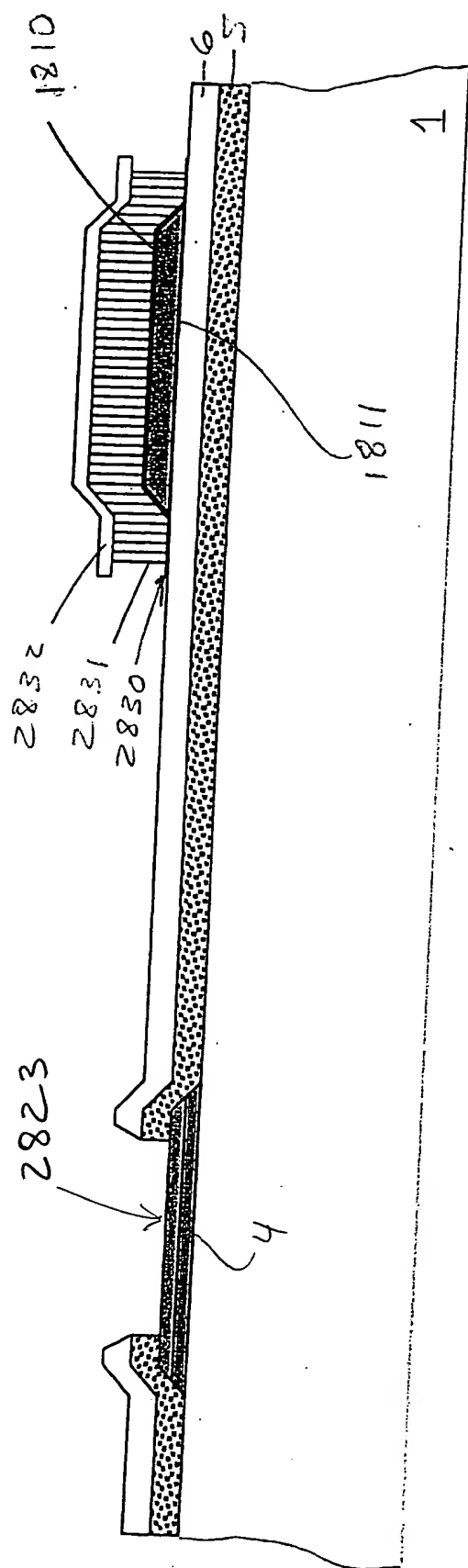
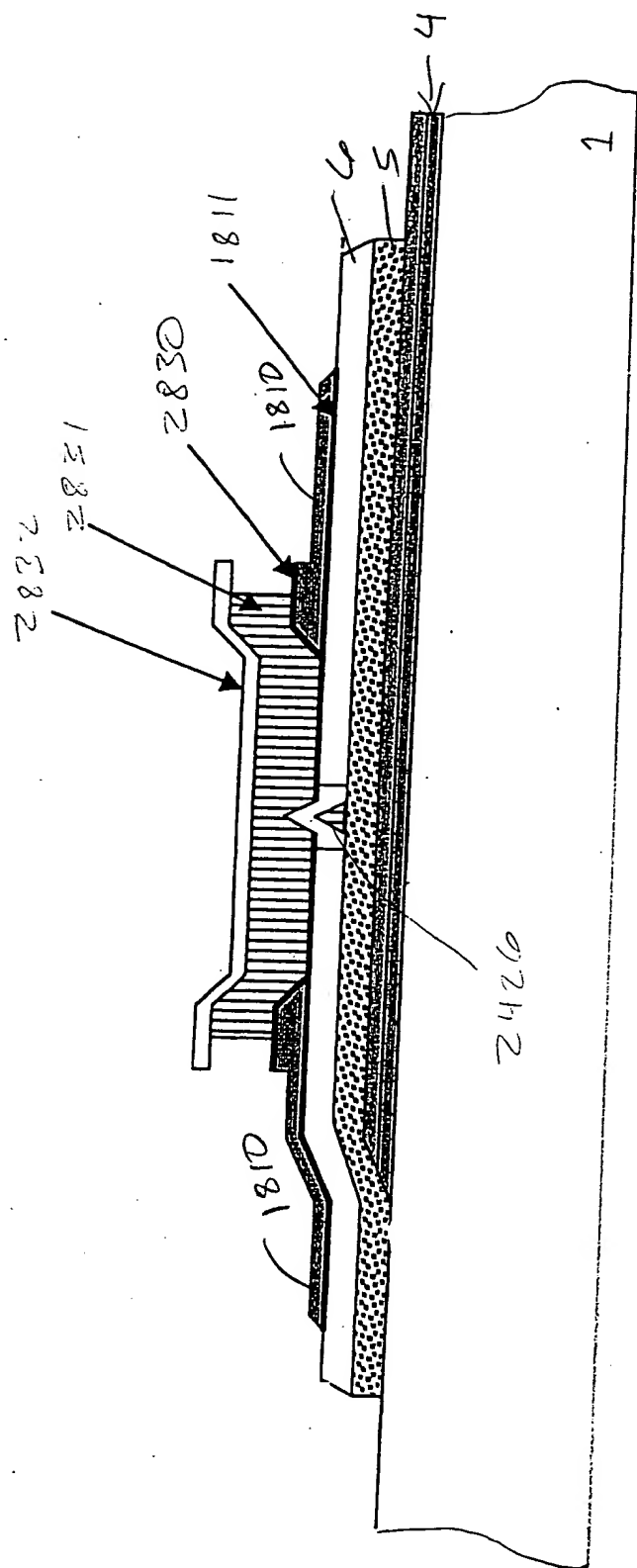
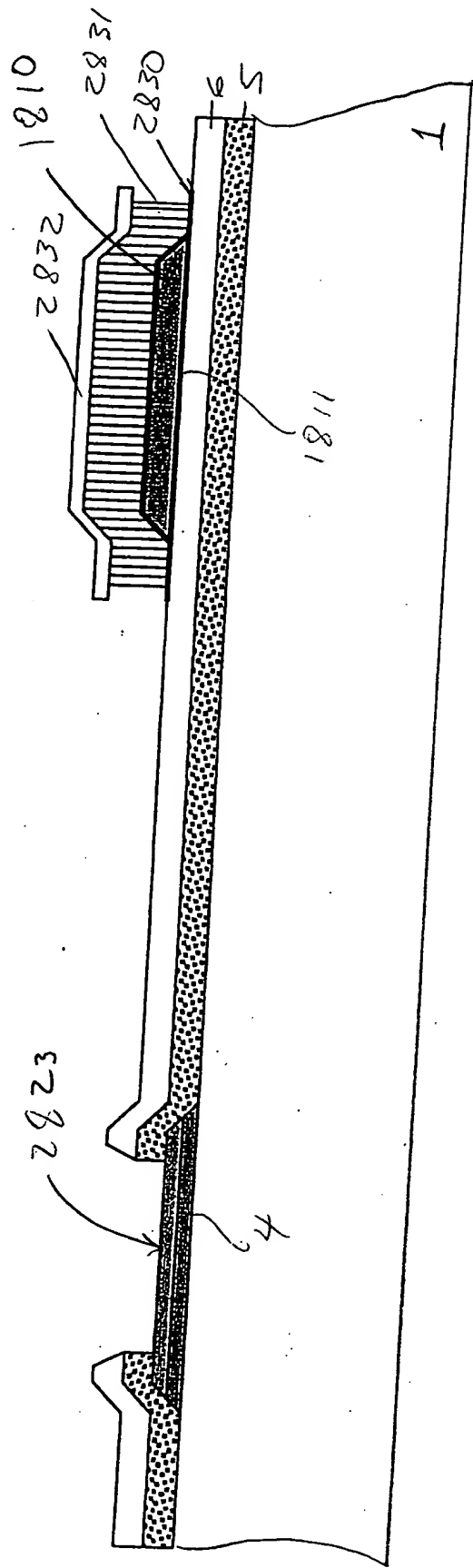
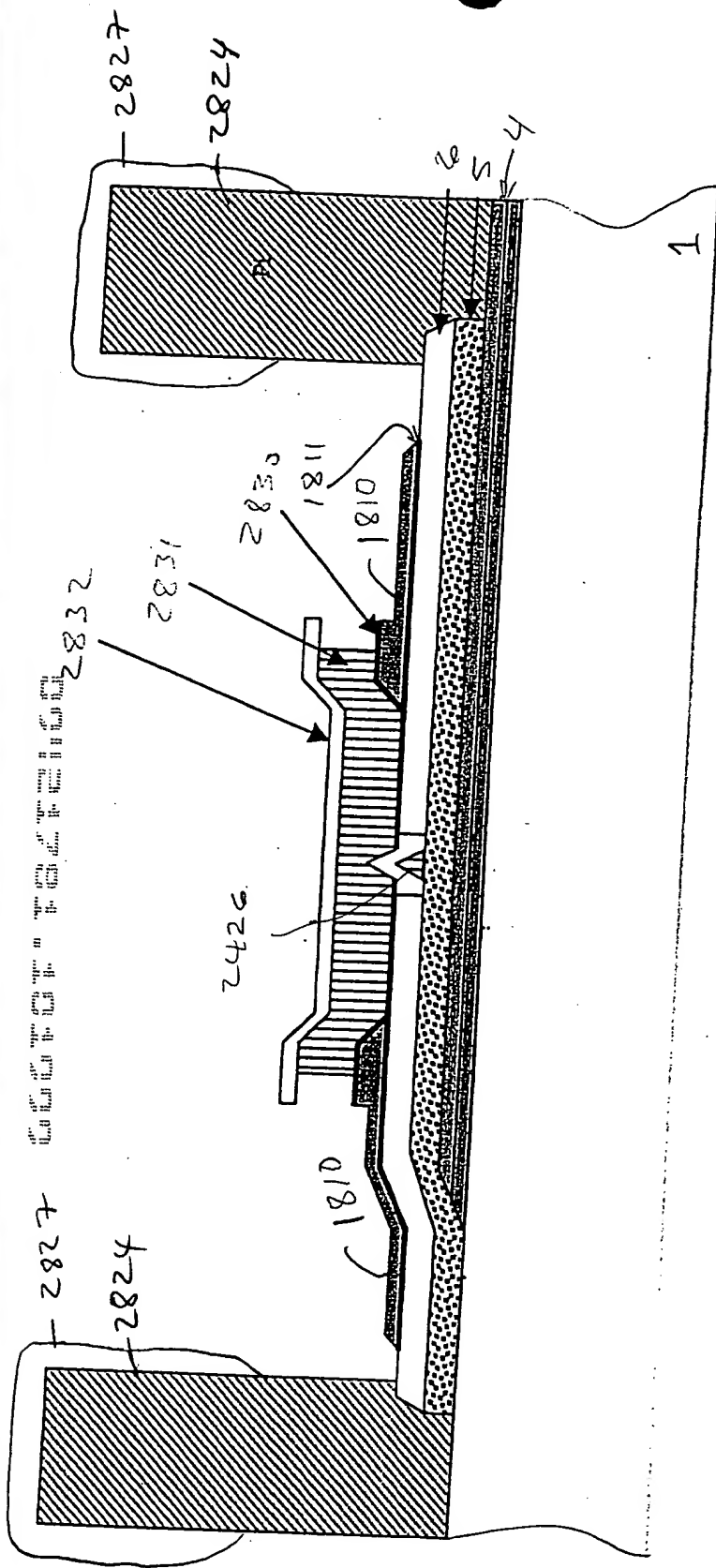
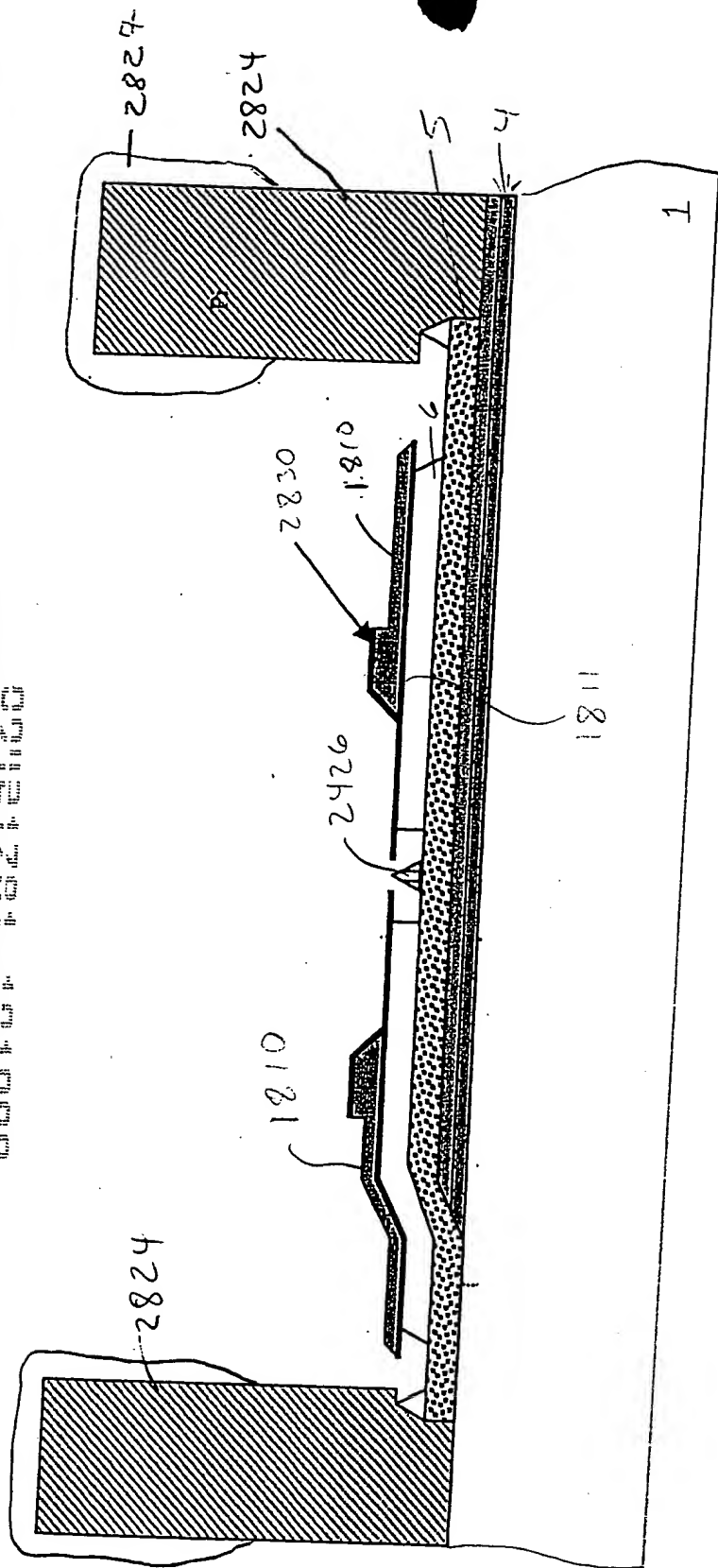


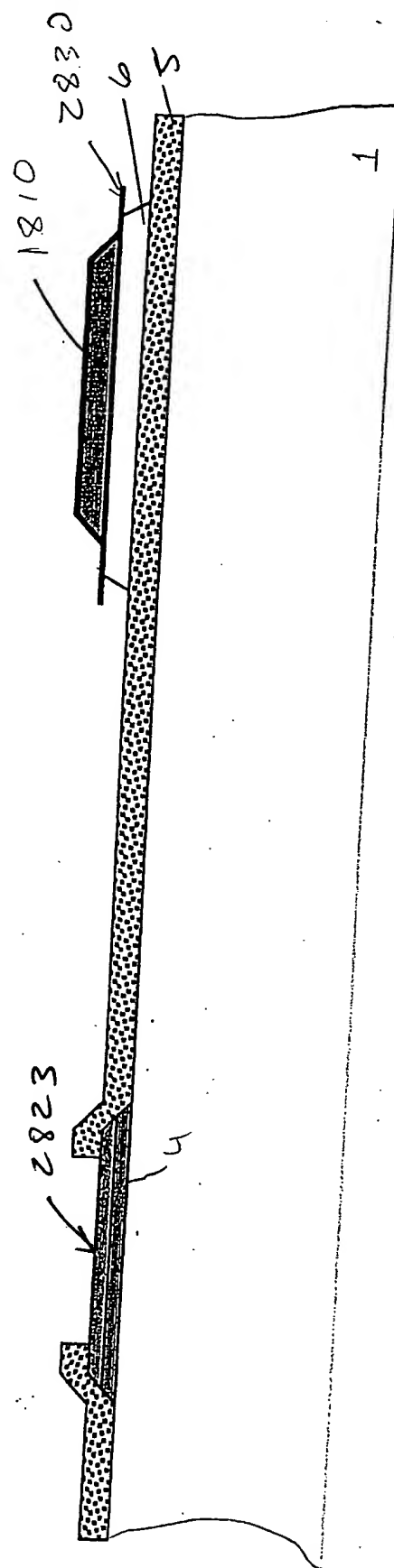
FIG 28D







78217



716282